

GENERAL DESCRIPTION

The DS33Z44 design kit is an easy-to-use evaluation board for the DS33Z44 Ethernet transport-over-serial link device. The DS33Z44DK is intended to be used with a resource card for the serial link. The serial link resource cards are complete with transceivers, transformers, and network connections. Dallas' ChipView software is provided with the design kit, giving point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal, queue overflow, Ethernet link, Tx/Rx, and interrupt status.

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ORDERING INFORMATION

PART	DESCRIPTION
DS33Z44DK	DS33Z44 demo card, T3/E3, T1/E1 transceiver resource card included

FEATURES

- Demonstrates Key Functions of DS33Z44 Ethernet Transport Chipset
- Includes Two Resource Cards: One with DS21458 T1/E1 SCT and one with DS3174 T3/E3 SCT, Transformers, BNC and RJ48 Network Connectors, and Termination
- Provides Support for Hardware and Software Modes
- On-Board MMC2107 Processor and ChipView Software Provide Point-and-Click Access to the DS33Z44 Register Set
- All DS33Z44 Interface Pins are Easily Accessible for External Data Source/Sink
- LEDs for Loss-of-Signal, Queue Overflow, Ethernet Link, Tx/Rx, and Interrupt Status
- Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs

DESIGN KIT CONTENTS

- DS33Z44DK Main Board
- Quad-Port Serial Card with DS21458 T1/E1 SCT
- Quad-Port Serial Card with DS3174 T3/E3 SCT
- CD_ROM
 - ChipView Software and Manual
 - DS33Z44DK Data Sheet
 - Configuration Files

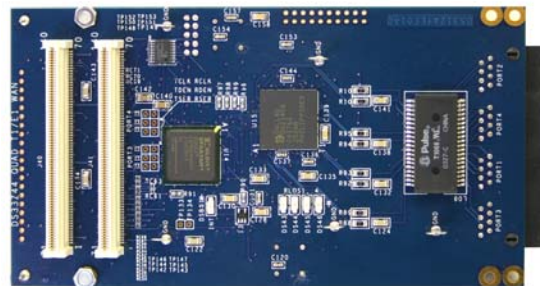
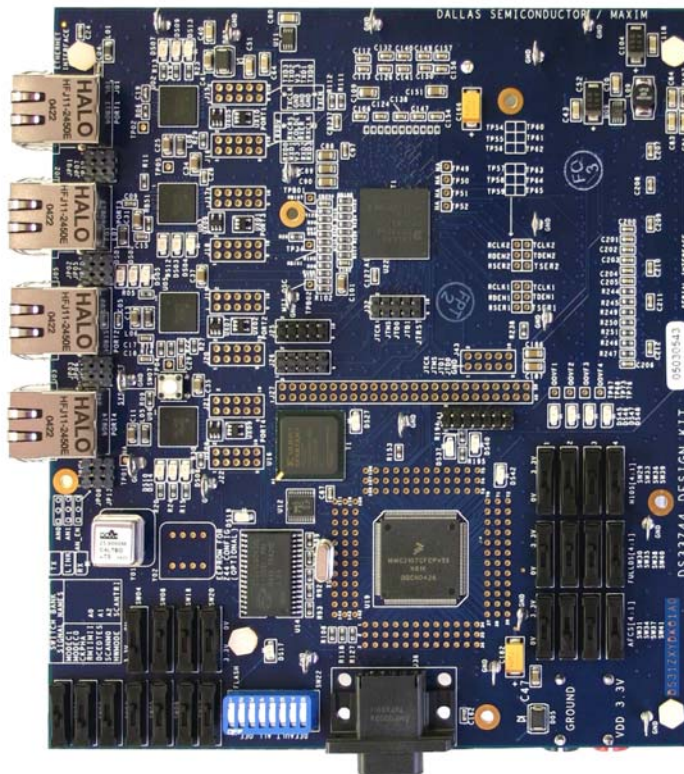


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COMPONENT LIST

[Table 1](#) shows the component list for the DS33Z44 and DS33Z11/DS33Z41 design kits and resource cards. This BOM contains the part listing for five boards. These boards are the DS33Z11DK, DS33Z44DK, DS21458RC, DS3174RC, and DS2155-DS21348-DS3170RC. Each reference designator is only used once. For example, U18 only appears on the DS33Z11DK and is not used on any of the other boards. See [Table 2](#).

Table 1. Component List (Decoupling Caps Not Shown)

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
U18	1	ELITE 10/100 ETHERNET TRANSPORT OVER SERIAL LINK 14X14 CSBGA 169 PIN	Dallas Semiconductor	DS33Z11
U20	1	3.3V T1.E1.J1 QUAD TRANSCEIVER 0-70C 256P BGA	Dallas Semiconductor	DS21458
U22	1	QUAD 10/100 ETHERNET EXTENSION TO WAN 17X17 PBGA 256 PIN	Dallas Semiconductor	DS33Z44
U23	1	DS3/E3 SCT, 11X11 CSBGA, 100 PIN	Dallas Semiconductor	DS3170
U24	1	T1/E1/J1 XCVR 100P QFP 0-70C	Dallas Semiconductor	DS2156L
U25	1	3.3V LIU	Dallas Semiconductor	DS21348
UB08	1	QUAD TRIPLE DUAL SINGLE ATM PACKET PHYS FOR DS3 E3 STS1 0-70C 400P BGA	Dallas Semiconductor	DS3184
U01, U09	2	SOIC 8PIN STEP-UP DC-DC CONVERTER 0.5A LIMIT	Maxim	MAX1675EUA
U07, U11	2	8-Pin μ MAX/SOIC 1.8V or Adj	Maxim	MAX1792EUA18
U13, UB01	2	MICROPROCESSOR VOLTAGE MONITOR, 2.93V RESET, 4PIN SOT143	Maxim	MAX811SEUS-T
U21, UB07	2	Dual RS-232 transceivers with 3.3V/5V internal capacitors	MAXIM	NA
U31, UB06, UB11	3	8-Pin μ MAX/SOIC 2.5V or Adj	Maxim	MAX1792EUA25
C11, C13, C16, C25, C27, C31–C35, C37, C41, C47, CB10, CB63, CB114, CB128, CB164, CB496	19	1206 CERAM 10uF 10V 20%	Panasonic	ECJ-3YB1A106M
CB390, CB391, CB395, CB396	4	1206 CERAM 0.1uF 25V 10%	Panasonic	ECJ-3VB1E104K
D01–D03, D05, DB03–DB05	7	SCHOTTKY DIODE, 1 AMP 40 VOLT	International Rectifier	10BQ040
DS01, DS07, DS10–DS12, DS17, DS20	7	LED, AMBER, SMD	Panasonic	LN1451C
DS02, DS03, DS09, DS14, DS15	5	L_LED, GREEN, SMD	Panasonic	LN1351C
DS04–DS06, DS08, DS13, DS16, DS18, DS27, DS28, DS35, DS37, DS38, DS40	13	LED, RED, SMD	Panasonic	LN1251C
DS19, DS43	2	LED, GREEN, SMD	Panasonic	LN1351C
DS21–DS26, DS30, DS32–DS34, DS36, DS39, DS41, DS42, DS44–DS48	19	L_LED, RED, SMD	Panasonic	LN1251C
GND_TP01–GND_TP07, GND_TP09–GND_TP44, GND_TP46–GND_TP68, GND_TPB01–GND_TPB10	76	STANDARD GROUND CLIP	KEYSTONE	4954
H1–H8, H17–H19	8	KIT, 4-40 HARDWARE, .50 NYLON STANDOFF AND NYLON HEX-NUT	NA	Lab Stock

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
H9-H16	16	KIT, 4-40 HARDWARE, 1.12 NYLON STANDOFF AND NYLON HEX-NUT (1.12 STANDOFF PN = 4807K-ND)	NA	Lab Stock
J01-J05	5	CONNECTOR, FASTJACK SINGLE, 8 PIN	Halo Electronics	HFJ11-2450E
J06, J41	2	100 MIL 2*7 POS JUMPER	NA	Lab Stock
J07-J12	6	RECEPTACLE, SMD, 140 PIN, .8MM, 2 ROW VERTICAL	AMP	5-179010-6
J13-J22	10	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT DO NOT POPLUATE	NA	Lab Stock
J23, J29, J32, J38, J39, J43, J44, J47, JB07	9	L_TERMINAL STRIP, SHROUDED, 10 PIN, DUAL ROW, VERT	3M Electronics	2510-6002UB
J24, J30, J31, J33	4	100 MIL 2 POS JUMPER	NA	Lab Stock
J25, J26, J45, J46	4	TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	NA	Lab Stock
J27, J42	2	CONN 50 PIN, 2 ROW, POSTS VERT, MOTHERBOARD FOOTPRINT	SAMTEC	TSW-125-07-T-D
J28, J36	2	L_CONN, DB9 RA, LONG CASE	AMP	747459-1
J48, J54, JB01	3	SOCKET, BANANA PLUG, HORIZONTAL, BLACK	Mouser Electronics	164-6218
J49-J52	4	CONNECTOR BNC 75 OHM VERTICAL 5PIN	Cambridge	CP-BNCP-004
J53, JB02, JB08	3	SOCKET, BANANA PLUG, HORIZONTAL, RED	Mouser Electronics	164-6219
J55, JB11	2	L_RJ48 8 PIN SINGLE PORT CONNECTOR	MOLEX	15-43-8588
J56-J59, J61, J63	6	CONNECTOR BNC 75 OHM RA 5PIN	Trompetor	UCBJR220
J60, J62, J64, J65	4	CONNECTOR BNC RA 5PIN	Trompetor	UCBJR220
JB05, JB06, JB09, JB10, JB13, JB14	6	PLUG, SMD, 140 PIN, .8MM, 2 ROW VERTICAL	AMP	179031-6
JB12	1	RA RJ45 8PIN 4PORT JACK	MOL	43223-8140
JP01-JP19	19	100 MIL 3 POS JUMPER	NA	NA
L01, L03-L08, LB01, LB02	9	FERRITE 3A 100 OHM AT 100 MHZ 1206 SMD	Steward	HI1206N101R-00
L02, L09	2	INDUCTOR 22.0uH 2PIN SMT 20%	Coiltronics	UP1B-220
L10	1	XFMR 1-2CT XMIT, 1-1CT RCV, 40P WIDE SOIC	Pulse	T1068
R01, R02, RB10, RB11, RB18, RB19, RB22, RB23, RB26, RB27	10	RES 0603 54.9 Ohm 1/16W 1%	Panasonic	ERJ-3EKF54R9V
R03, R04, RB12, RB13, RB20, RB21, RB24, RB25, RB28, RB29	10	RES 0603 49.9 Ohm 1/16W 1%	Panasonic	ERJ-3EKF49R9V
R05, R06, R08, R09, R11	5	RES 0603 10.0K Ohm 1/16W 1% - Must be 1% tolerance	Panasonic	ERJ-3EKF1002V
R07, R12, R16, R79, R160, R244, R248, R250, R251, R254, R255, RB126, RB143, RB147, RB150, RB157	16	RES 0603 1.0K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ102V
R10, R107	2	RES 1206 5.6 Ohm 1/8W 5%	Panasonic	ERJ-8GEYJ5R6V
R132, R137, R142, R144, R156, RB194, RB208, RB227	8	L_RES 0603 0 Ohm 1/16W 1%	AVX	CJ10-000F

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R13–R15, R18–R20, R22, R23, R29, R30, RB01, RB03, RB07, RB09, RB15–RB17, RB30–RB32, RB34–RB38, RB41, RB44, RB47, RB48, RB50–RB52, B55, RB60, RB62, RB72, RB73, RB75, RB80, RB82	40	RES 0603 5.1K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ512V
R17, R21, R25–R28, R31, R55, R57–R59, R71, R74–R76, R83, R96–R102, R105, R106, R109, R111, R112, R115–R117, R120, R122–R126, R128, R133, R134, R140, R141, RB61, RB96, RB97, RB99, RB100, RB102–RB110, RB112, RB114–RB119, RB121, RB123–RB125, RB127, RB128, RB130, RB131, RB133, RB135–RB138, RB145, RB148, RB149, RB160, RB161, RB164, RB165, RB167–RB171, RB173–RB181, RB184, RB187, RB311, RB320, RB335, RB339, RB359	104	RES 0603 30 Ohm 1/16W	Panasonic	ERJ-3GEYJ300V
R171, R172, R174, R175, R190, R191, R240, R241	8	L_RES 0805 0.0 Ohm 1/10W 5%	Panasonic	ERJ-6GEY0R00V
R198–R200, R210–R213, RB306, RB325, RB326	10	RES 0603 332 Ohm 1/16W 1%	Panasonic	ERJ-3EKF3320V
R201–R208, RB321–RB324, RB327–RB330	16	RES 1206 0 Ohm 1/8W 5%	Panasonic	ERJ-8GEYJ0R00V
R239, RB349	2	RES 0805 51.1 Ohm 1/10W 1%	Panasonic	ERJ-6ENF51R1V
R24, R114, R197, RB14, RB33, RB40, RB42, RB43, RB49, RB53, RB54, RB57–RB59, RB71, RB77, RB78, RB152–RB156, RB221, RB234, RB251, RB284, RB304, RB331, RB332, RB342, RB344, RB350, RB354, RB360	34	L_RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V
R242, R243, RB144, RB166, RB355–RB358, RB368–RB371	12	RES 0603 51 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ510V
R32, R70, R78, R161, R176, R194, R195, R237, R238, RB129, RB134, RB146, RB193	13	RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V
R33–R54, R60–R69, R72, R73, R131, R136, R143, R147, R150, R154, R158, R163, R166, R169, R173, R178–R189, R215–R228, RB89–RB95, RB101, RB188–RB191, RB196–RB199, RB202–RB205, RB210–RB213, RB216–RB219, RB223–RB226, RB230–RB233, RB239–RB242, RB244–RB249, RB252–RB260, RB265–RB268, RB270–RB282, RB289–RB297	152	RES 0402 30 Ohm 1/16W 5%	Panasonic	ERJ-2GEJ300X
R56, R90	2	RES 0603 1.0M Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ105V
R77, RB159	2	L_RES 1206 0 Ohm 1/8W 5%	Panasonic	ERJ-8GEYJ0R00V
R80, R81, R84, R87, R89, R91–R93, R95, R108, R110, R118, R127, R152, R153, R196, R209, R214, R229–R236, RB200, RB237, RB238, RB263, RB264, RB286, RB287, RB300, RB301, RB333, RB364	37	RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R85, R88, R94, R104, R113, RB02, RB04-RB06, RB08, RB39, RB45, RB46, RB56, RB63-RB70, RB76, RB83, RB98, RB183, RB185, RB192, RB209, RB228, RB302, RB303, RB305, RB338, RB340, RB341, RB346-RB348, RB351-RB353, RB361-RB363, RB365-RB367	48	RES 0603 2.0K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ202V
R86, R103, R119, R121, R129, R130, R135, R138, R139, R145, R146, R149, R151, R157, R162, R164, R167, R168, R170, R177, R192, R193, R245-R247, R249, R252, R253, R256, R257, RB74, RB79, RB132, RB139-RB141, RB151, RB162, RB163, RB172, RB182, RB186, RB206, RB207, RB214, RB215, RB220, RB222, RB229, RB235, RB236, RB243, RB250, RB261, RB262, RB269, RB308-RB310, RB343, RB345	61	L_RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V
RB201, RB285	2	RES 0805 330 Ohm 1/10W 5%	Panasonic	ERJ-6GEYJ331V
RB283	1	RES 0603 10K Ohm 1/10W 5% - SEE SPECIAL INSTRUCTIONS	Panasonic	603_ERJ-3GEYJ103V
RB298, RB299, RB312-RB319, RB336, RB337	12	RES 0805 61.9 Ohm 1/10W 1%	Panasonic	ERJ-6ENF61R9V
RB81, RB84-RB88, RB111, RB113, RB120, RB122	10	RES 0603 DO NOT POPULATE	NA	NA
SW01-SW05, SW08-SW21, SW24-SW26, SW29-SW31, SW33-SW44	37	L_SWITCH, SP3T SLIDE, 4PIN TH	Tyco	3-1437575-3
SW06, SW22	2	L_SWITH 8POS 16PIN DIP LOW PROFILE	AMP	435668-7
SW07, SW23	2	SWITCH MOM 4PIN SINGLE POLE	Panasonic	EVQPAE04M
SW27, SW28, SW32	3	L_DIPSWITCH, 10 POS	AMP	435668-9
T01, T03	2	XFMR 16P SMT	Pulse	TX1099
T02, TB01	2	XFMR, OCTAL T3/E3, 1 TO 2, SMT 32 PIN	Pulse	T3049
TP01-TP78, TPB01, TPB02	80	TESTPOINT, 1 PLATED HOLE, DO NOT STUFF	NA	NA
U02-U06	5	IC, DsPHYTER11-SINGLE 10/100 ETHERNET TRANSCEIVER, 65 PIN LLP	National Semiconductor	DP83847ALQA5 6A
U08, U12, U29	3	1MBit Flash based config mem	Avnet	XCF01SV020C
U10	1	XILINX SPARTAN xc200 2.5V FPGA,256 PIN BGA	Xilinx	XC2S200-5FG256C
U14, U26, U30, UB05	4	CYPRESS SRAM, LAB STOCK	NA	NA
U15, U19	2	mmc2107 processor	Motorola	MMC2107
U16, U27	2	XILINX SPARTAN 2.5V FPGA,256 PIN BGA	Xilinx	XC2S50-5FG256C
U17, U28, U32	3	10 pin res pack, 10K ohm	NA	NA
UB02, UB03, UB04	3	100 PIN CPLD	XILINX	XC95144XL-10TQ100C
UB09, UB10	2	SYNCHRONOUS DRAM, 1MEGX32X4 BANKS, TSOP 86 PIN	Micron	MT48LC4M32B2 TG-7

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
UX01-UX12, UXB02-UXB04, UXB06-UXB08	18	HIGH SPEED BUFFER	Fairchild	NC7SZ86
UXB01, UXB05	2	HIGH SPEED INVERTER	Fairchild	NC7SZ86
X01, X02	2	XTAL LOW PROFILE 8.0MHZ	ECL	EC1-8.000M
Y01, Y09	2	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 25.000 MHZ, Low Jitter required for PHY	SaRonix	NTH089AA3- 25.000
Y02, Y13	2	SPI SERIAL EEPROM 16K 8 PIN DIP 2.7V NEEDS SOCKET	Atmel	AT25160A-10PI- 2.7
Y03	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 2.048 MHZ	SaRonix	NTH039A3- 2.0480
Y05, Y06	2	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 100.000 MHZ	SaRonix	NTH089A3- 100.0000
Y07	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 44.736 MHZ	SaRonix	NTH089AA3- 44.736
Y08	1	OSCILLATOR, CRYSTAL CLOCK, 5.0V - 44.736 MHZ	SaRonix	NTH089AA- 44.736
YB02	1	L_OSCILLATOR, CRYSTAL CLOCK, 3.3V - 2.048 MHZ	SaRonix	NTH039A3- 2.0480

Figure 1. System Floorplan

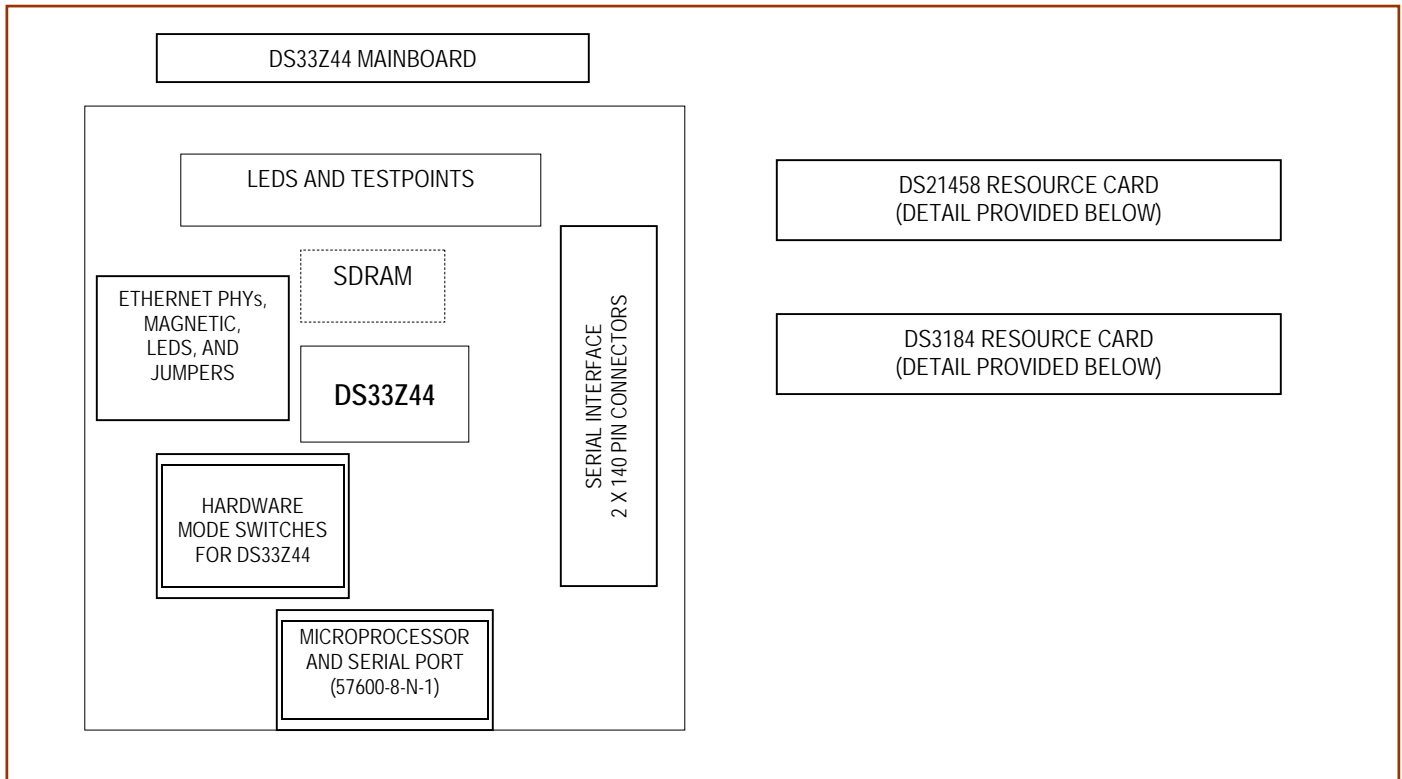
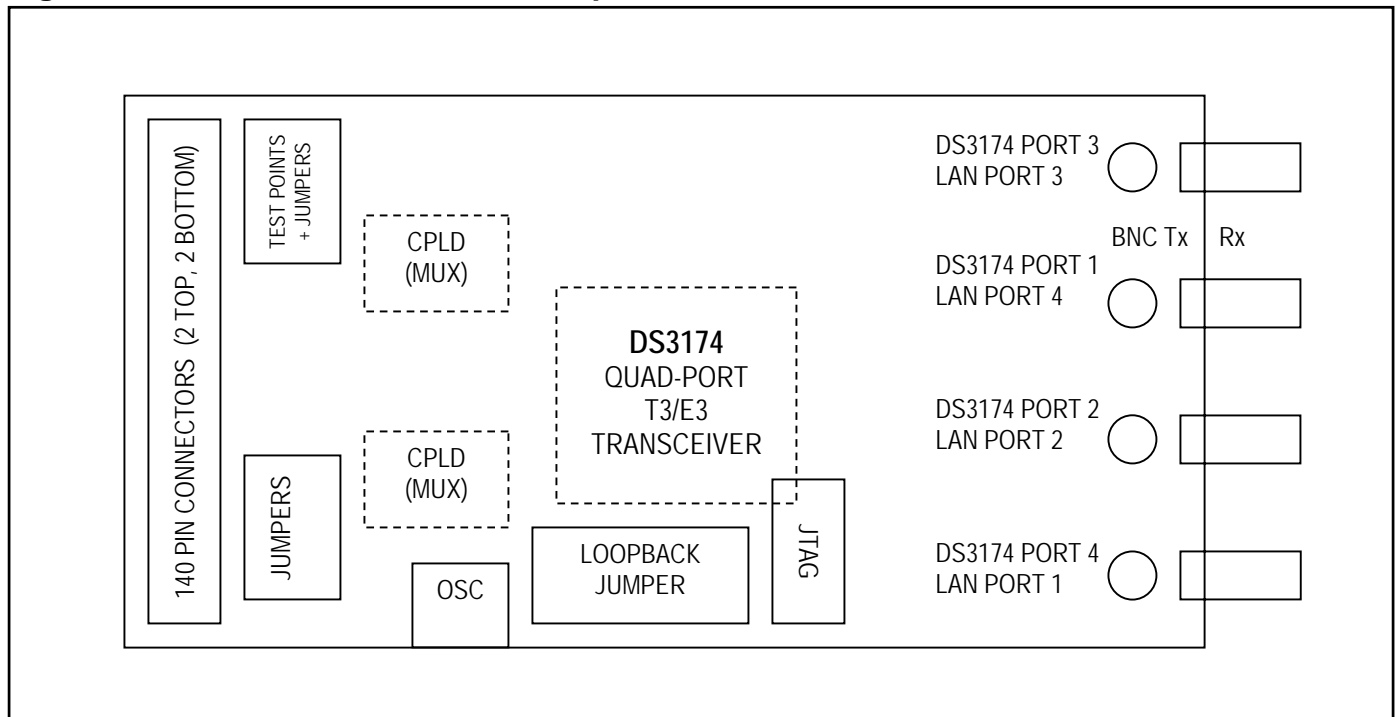


Figure 2. DS3174 Resource Card Floorplan



The DS3174 quad T3/E3 PC board floorplan is shown in [Figure 2](#). Jumpers JP16, JP17, JP18, and JP19 are 3-pin jumpers used to tri-state/enable T3/E3 ports. With the board oriented as shown in Figure 2, the top 2 pins of each jumper would be connected to enable T3/E3 traffic.

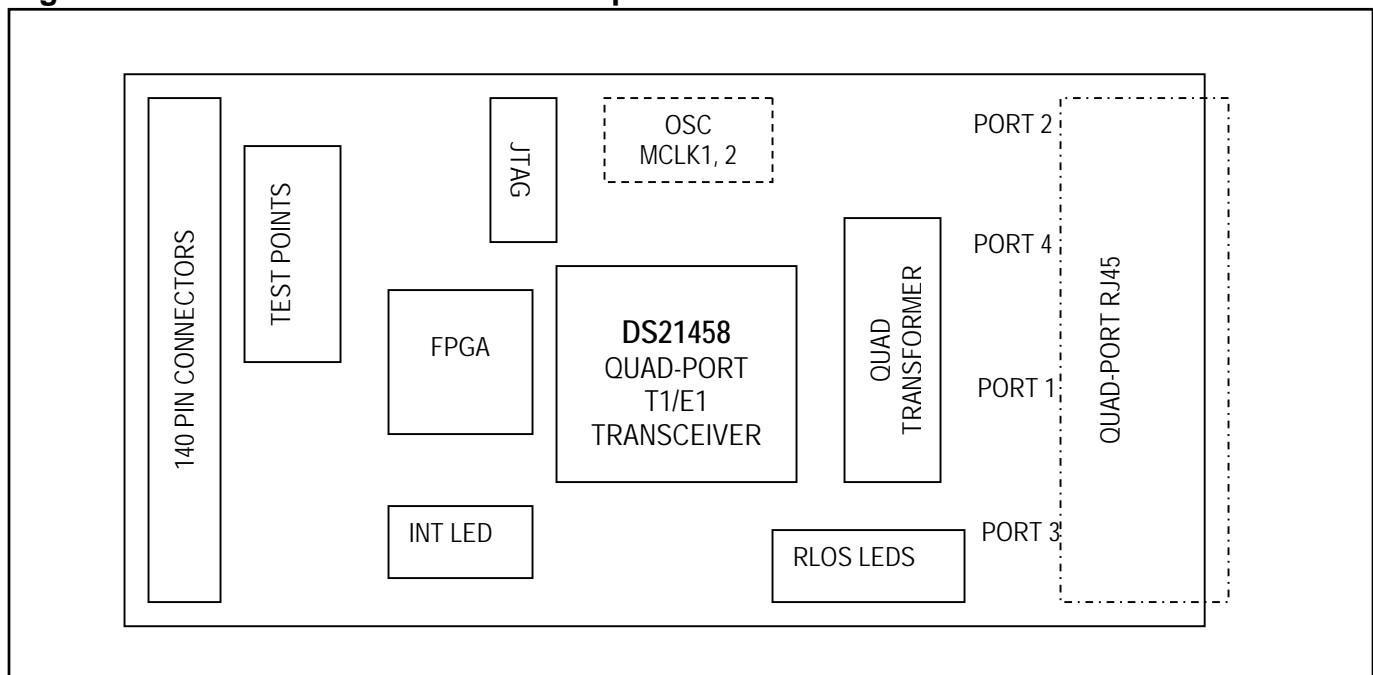
A 2-pin jumper, JP24, has been added to allow loopback. When installed, the board is in loopback at the CPLD; all traffic sent by the DS33Z44 is then sent back to the Z44. Traffic sent by the DS3174 is ignored in CPLD loopback mode.

The quad T3/E3 board is intended to be connected to the DS33Z11 or DS33Z44 motherboards. The quad T3/E3 board can be used with the quad T1/E1 board. When used in this manner, the quad T1/E1 board is stacked underneath the quad T3/E3 board. Jumpers on the T3/E3 board are then used to tri-state or enable individual ports on either board.

[Figure 3](#) shows the DS21458 quad T1/E1 PC board floorplan. The current configuration is to populate oscillators for MCLK1 with a 2.048MHz oscillator. Testpoints for port 3 and port 4 are provided on the WAN card, and testpoints for ports 1 and 2 are provided on the motherboard.

The quad T1/E1 board can be used with the quad T3/E3 board. When used in this manner, the quad T1/E1 board is stacked underneath the quad T3/E3 board. Jumpers on the T3/E3 board are then used to tri-state or enable individual ports on either board.

Figure 3. DS21458 Resource Card Floorplan



PC BOARD ERRATA

- Silk screen for the serial resource card has V_{CC} and ground indicators pointing the wrong direction for configuration switches SW27, SW28, and SW32. This should be corrected with an adhesive label.
- Signal descriptions for JTAG connector are incorrect on the Quad T1E1 card. This should be corrected with an adhesive label.
- In the PCB layout the transformer TX primary is on the wrong side (creating a 2:1 winding instead of a 1:2). This has been corrected in the schematic, the PCB / assembly has been modified to correct this.

FILE LOCATIONS

This design kit relies upon several supporting files, which are provided on the CD and are available as a zip file from the Maxim website at www.maxim-ic.com/DS33Z44DK.

All locations are given relative to the top directory of the CD/zip file.

- DS33Z44 register definition files and configuration files:
 - `.\cfg_demo_gui\DS33Z44_cfg_demo_gui\DS33Z44.def`
 - `.\DS33Z44_cfg_demo_gui\SU_LI_PORT4.def` (def files for port 3, 2, 1 not shown)
 - `.\DS33Z44_cfg_demo_gui\basic_config.mfg`
- DS21458 register definition files and configuration files:
 - `.\DS33Z44_cfg_demo_gui\Qt1e1_DS21458\DS21458RC.def`
 - `.\DS33Z44_cfg_demo_gui\Qt1e1_DS21458\DS21458RC_FPGA.def`
 - `.\DS33Z44_cfg_demo_gui\Qt1e1_DS21458\e1_gapclk_crc4_hdb3_nocas.ini`
 - `.\DS33Z44_cfg_demo_gui\Qt1e1_DS21458\gapclk_DS21458_T1_ESF_LBO0.ini`
- DS3174 register definition files and configuration files:
 - `.\DS33Z44_cfg_demo_gui\Qt3e3_DS3184\ds3184_evbrd_reduced.def`
 - 14 other low level def files
 - `.\DS33Z44_cfg_demo_gui\Qt3e3_DS3184\84_t3_sct_needscoaxlb.mfg`

BASIC OPERATION

Powering Up the Design Kit

- Attach resource card to main board.
- Connect PCB 3.3V and GND banana plugs to power supply. At power-up the system should draw approximately 1A.
- Set switches for software mode as described in [Table 2](#) (short description follows).
 - Top left bank: All low, except for MODEC0, which is high.
 - Top right bank: A2, A1, A0 in mid position, SCANTRI low
 - Bottom Bank: All high (AFCS, FULLDS, H1OS)

General

- Upon power-up, the processor FPGA Status LEDs (DS19 green) will be lit. Interrupt LEDs (DS42 red) will not be lit. DS33Z44 Queue overflow LEDs (DS45, DS46, DS47, DS48 red) will not be lit. PHY LINK LED (DS02, DS03, DS14 green) should be lit if the Ethernet is connected.

Following are several basic system initializations.

Basic DS33Z44 Initialization (Used for All Quick Setups)

This section covers four basic methods for configuring the Z44. Any one of these initializations can be used with the following Quick Setup examples:

1. Upon power-up, the on-board device driver provides a basic configuration for the DS33Z44 and attached serial cards. This enables traffic to pass from the Ethernet port to the serial port. Consult the device driver documentation for further details. Device driver behavior is dependant upon jumper settings, which are detailed in Table 2.
2. Register-Based Configuration. Launch ChipView.exe and select *Register View*. When prompted for a definition file, pick the file named **DS33Z44.def**. After the definition file loads, go to the File menu and select *File*→*Memory Config File*→*Load* .MFG file. When prompted, select the file named **4Portsbasic_config.mfg**.
3. Hardware Mode. Set switches as described in the section for powering up the design kit, then change the following: HWMODE←3.3V, A0←3.3VV, A1←3.3V, A2←0V. This sets the part for LSB first, scrambling off, HDLC encapsulated. At this point traffic will pass from the Ethernet port to the serial port. In this mode broadcast frames are not passed (i.e., ping).
4. EEPROM mode is available with the DK, but is beyond the scope of this manual.

Quick Setup #1 (Device Driver + CPLD Loopback)

- On the serial resource card install jumper 24. Jumpers JP16–JP19 should be set high. This places the card in CPLD loopback and enables all four ports as described in [Table 3](#).
- Complete the hardware configuration and one of the basic DS33Z44 configurations as described in the previous section.
- Using a patch cable, connect the Ethernet connector to an ordinary PC, or network test equipment. This should cause the link LED to turn on.
- At this point any packets sent to the DS33Z44 are echoed back. Incoming packets (i.e., ping) should cause the RX LED to blink, after which the TX LED should also blink.
- To interact with the device driver select from the drop down menu:
 - Tools→Plugins→Load Plugins. When asked if DLLs have already registered select yes
 - Select Tools→Plugins→DS33Z44/11/41 Device Driver Demo
 - A new form called 'Zchip Configuration' pops up.
 - Preload basic configuration for the GUI by selecting File→Load Settings (in the 'Zchip Configuration' form). Select the file named 'basic_Config.eset'

Quick Setup #2 (DS3174 T3E3)

- On the DS3174 serial resource card install jumper J24. Jumpers JP16–JP19 should be set high. This places the card in DS3174 mode and enables all four ports as described in [Table 3](#).
- Complete the hardware configuration and one of the basic DS33Z44 configurations as previously described.
- Using a patch cable, connect the Ethernet connector to an ordinary PC, or network test equipment. This should cause the link LED to turn on.
- Launch ChipView.exe (or use existing session if it is already open) and select *Register View*. When prompted for a definition file, pick the file name **ds3184_evbrd_reduced.def**. After the definition file loads, go to the File menu and select **File→Memory Config File→Load .MFG file**. When prompted, select the file named **84_t3_sct_needscoaxlb.mfg**.
- Place a loopback connector at the DS3174 network side.
- At this point, any packets sent to the DS33Z44 are echoed back. Incoming packets (i.e., ping) should cause the RX LED to blink, after which the TX LED should also blink.

Quick Setup #3 (DS21458 T1E1)

- Complete the hardware configuration and one of the basic DS33Z44 configurations as previously described.
- Using a patch cable, connect the Ethernet connector to an ordinary PC, or network test equipment. This should cause the link LED to turn on.
- Launch ChipView.exe (or use existing session if it is already open) and select *Register View*. When prompted for a definition file, pick the file named **DS21458.def**. After the definition file loads, go to the File menu and select **File→Reg Ini File→Load Ini File**. When prompted, pick the file named **e1_gapclk_crc4_hdb3_nocas.ini**.
- Place a loopback connector at the DS21458 network side; RLOS LED should go out.
- At this point any packets sent to the DS33Z44 are echoed back. Incoming packets (i.e. ping) should cause the RX LED to blink, after which the TX LED should also blink.

CONFIGURATION SWITCHES AND JUMPERS

The DS33Z44DK has several configuration switches, banana plugs, oscillators, and jumpers. [Table 2](#) provides a description of these signals, given in order of appearance on the PC board (going from left to right, top to bottom).

Table 2. Main Board PC Board Configuration

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING		DESCRIPTION
		SW MODE	HW MODE	
J25.9 + J25.10	Reserved	Not Installed	—	This jumper is not for use with the DS33Z44 design kit. Pin J25.10 has been removed to prevent accidental installation.
J25.7 + J25.8	Enable device driver	User decision	—	When installed the device driver will configure the DS33Z44 and the Transceiver during power-up.
J25.5 + J25.6	Enable callbacks	User decision	—	When installed the driver will respond to interrupts.
GROUND (banana plug)	Power supply ground	—	—	System Ground. Always connected to power supply.
VDD 3.3V (banana plug)	Power supply VDD	—	—	System VDD. Always connected to power supply.
OnCe	BDM	—	—	Debug connector for processor
DCEDTES (3pos switch)	DS33Z44 mode pin; DTE/DCE selection	Low	Low	Low for DTE
RMII MII (3pos switch)	DS33Z44 mode pin	Low	Low	High for RMII, low for MII
CKPHA (3pos switch)	DS33Z44 mode pin	Low	Low	SPI EEPROM hardware mode configuration switch
MODEC0 (3pos switch)	DS33Z44 mode pin	High	Low	Software mode selected
MODEC1 (3pos switch)	DS33Z44 mode pin	Low	Low	Software mode selected
HWMODE (3pos switch)	DS33Z44 mode pin	Low	Low	Hardware/software mode (software mode selected)
SCANMO (3pos switch)	DS33Z44 mode pin	Low	Low	Set low for normal operation
SCANTRI (3pos switch)	DS33Z44 mode pin	Low	Low	Set low for normal operation
...testpoints....	DS33Z44 testpoints	—	—	Processor bus, JTAG and LAN side testpoints for Zchip
Z-RESET (button)	DS33Z44 reset	—	—	System reset
A2, A1, A0 (3pos switches)	DS33Z44/SPI pins	Mid position	Mid position	Address pin/EEPROM config switch. Set to mid position to allow connection to processor.
SDRAM CLOCK	DS33Z44 SDRAM clock	Installed	Installed	100MHz oscillator to drive SDRAM clock
MII CLOCK	PHY MII clock	Installed	Installed	25MHz oscillator to drive SDRAM clock
spi_cs, spi_ck, spi_miso, spi_mosi	—	—	—	SPI signals (for EEPROM memory)
...testpoints.....	DS33Z44 testpoints	—	—	DS33Z44 serial port testpoints
AFCS (1 per port)	DS33Z44 mode pin	HW mode only	High	Set high to enable auto flow control.

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING		DESCRIPTION
		SW MODE	HW MODE	
FULLDS (1 per port)	DS33Z44 mode pin	HW mode only	High	Set high to enable full duplex.
H10S (1 per port)	DS33Z44 mode pin	HW mode only	High	Set high to config for 100Mb.
GROUND/VDD (banana plug)	Power supply ground/3.3V	—	—	Redundant connection to system power. Use plugs at either top or bottom of board.
VDD 3.3V (banana plug)	Power supply VDD	—	—	Redundant connection to system power. Use plugs at either top or bottom of board.

Table 3. DS3174 Serial Reference Card Jumper Settings

JUMPER SETTINGS	MODE	COMMENT
JP16	Port 4 tri-state (at CPLD)	When the middle pin of this 3 position jumper is set to VCC, the CPLD passes traffic from the DS3174 to the DS33Z44. When the pin is set low, the CPLD tri-states this port.
JP17	Port 2 tri-state (at CPLD)	When the middle pin of this 3 position jumper is set to VCC, the CPLD passes traffic from the DS3174 to the DS33Z44. When the pin is set low, the CPLD tri-states this port.
JP18	Port 3 tri-state (at CPLD)	When the middle pin of this 3 position jumper is set to VCC, the CPLD passes traffic from the DS3174 to the DS33Z44. When the pin is set low, the CPLD tri-states this port.
JP19	Port 1 tri-state (at CPLD)	When the middle pin of this 3 position jumper is set to VCC, the CPLD passes traffic from the DS3174 to the DS33Z44. When the pin is set low, the CPLD tri-states this port.
J243	CPLD loopback	CPLD loopback makes the following connections: Zrser ← Ztser, Ztden ← 3.3V, Zrden ← 3.3V, Ztclki ← OscY03, Zrclki ← OscY03

ADDRESS MAP (ALL CARDS)

Motorola resource card address space begins at 0x81000000. All offsets given below are relative to the beginning of the daughter card address space (shown previously).

Table 4. Overview of Daughter Card Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0087	FPGA	Processor board identification
0X1000 to 0X1FFF	DS33Z44	DS33Z44. Uses CS_X1.
0X2000 to 0X2FFF	DS21458	T1E1 DS21458 resource card. Uses CS_X2.
0X4000 to 0X4010	FPGA	FPGA on DS21458 resource card. Used to facilitate IBO mode. Default configuration of FPGA is compatible with non-IBO mode functionality. The FPGA settings do not require modification for use with the DS33Z44.
0X3000 to 0X3FFF	DS3174	T3E3 resource card. Uses CS_X3.

Registers in the DS33Z44, DS21458, and DS3174 can be easily modified using the ChipView host-based user-interface software with the definition files previously mentioned.

DS33Z44 INFORMATION

For more information about the DS33Z44, consult the DS33Z44 data sheet available on our website at www.maxim-ic.com/DS33Z44.

DS33Z44DK INFORMATION

For more information about the DS33Z44DK, including software downloads, consult the DS33Z44DK data sheet available on the our website at www.maxim-ic.com/DS33Z44DK.

TECHNICAL SUPPORT

For additional technical support, go to www.maxim-ic.com/support.

DOCUMENT REVISION HISTORY

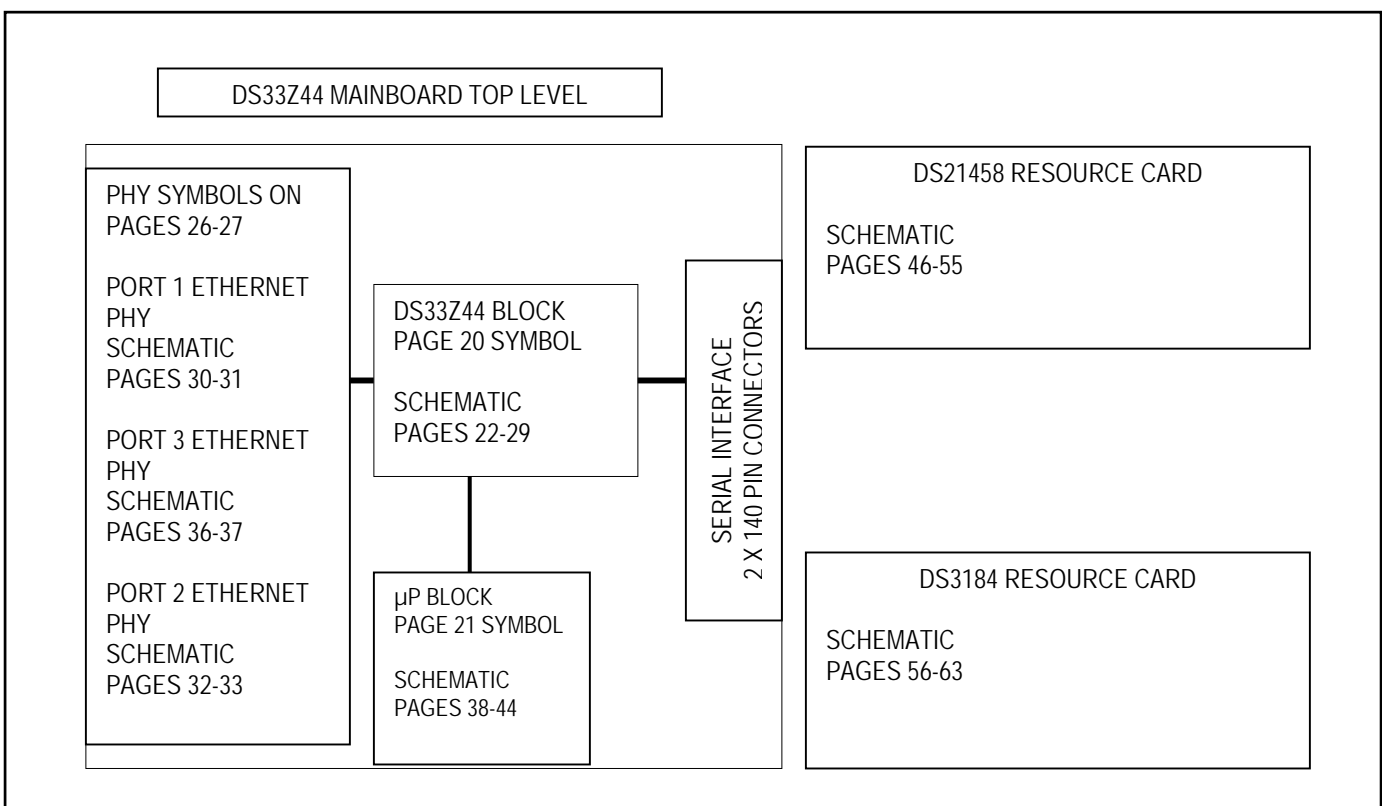
REVISION DATE	DESCRIPTION
032305	Initial DS33Z44DK data sheet release.
042205	Updated <i>Basic DS33Z44 Initialization</i> section; added step to <i>Quick Setup #1</i> .
051105	Added new PC board errata.
110106	Updated schematics.

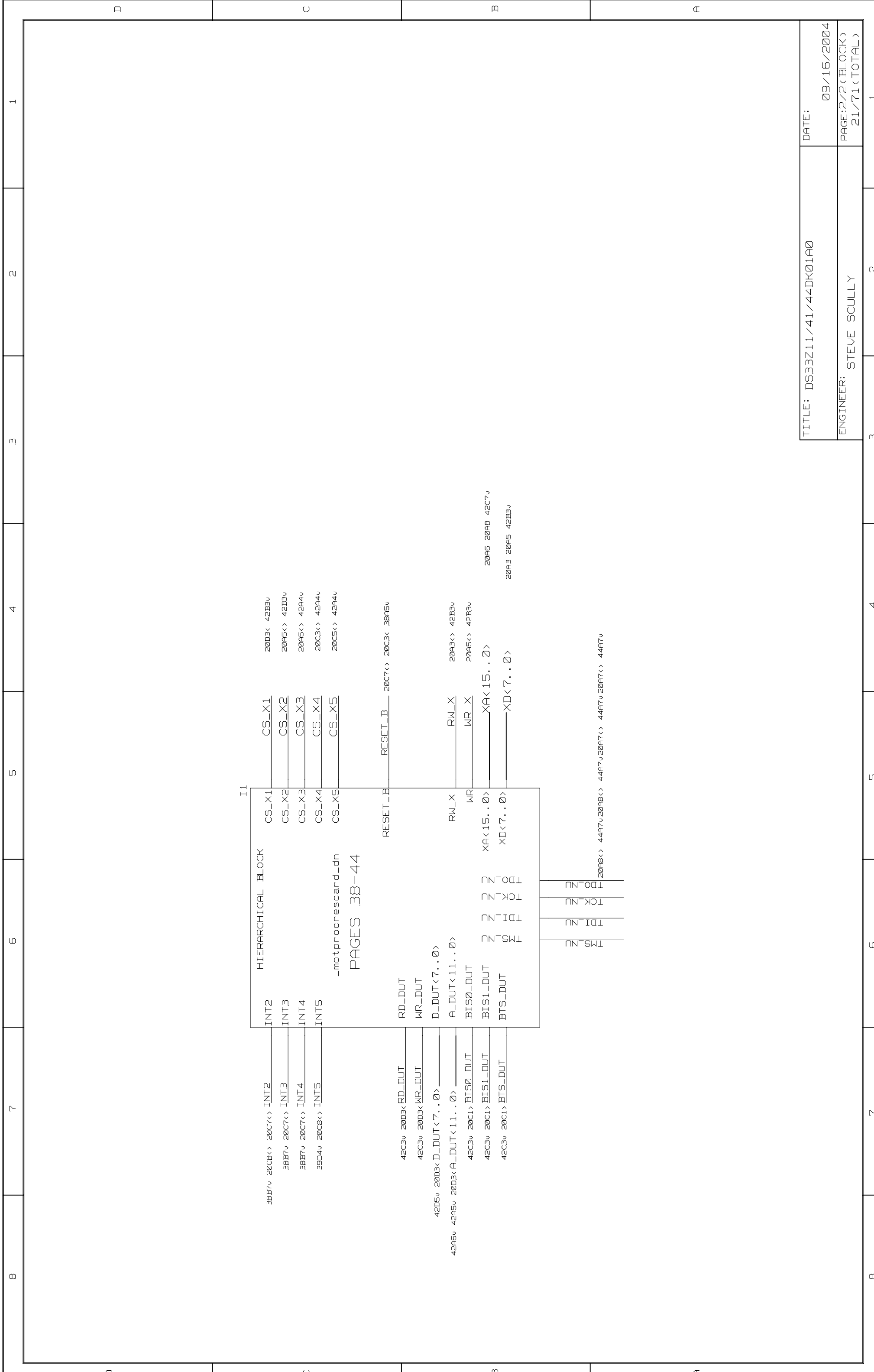
SCHEMATICS

The DS33Z44DK schematics are featured in the following pages. As this is a hierarchal schematic some explanation is in order. The main board is composed of six hierarchal blocks: the processor block, the DS33Z44 block, and four Ethernet blocks inside the DS33Z44 block, which is a nested hierarchy block. Each serial card (DS21458 and DS3174) consists of a single hierarchy block, which connects to a 140-pin AV bus that snaps into the mainboard.

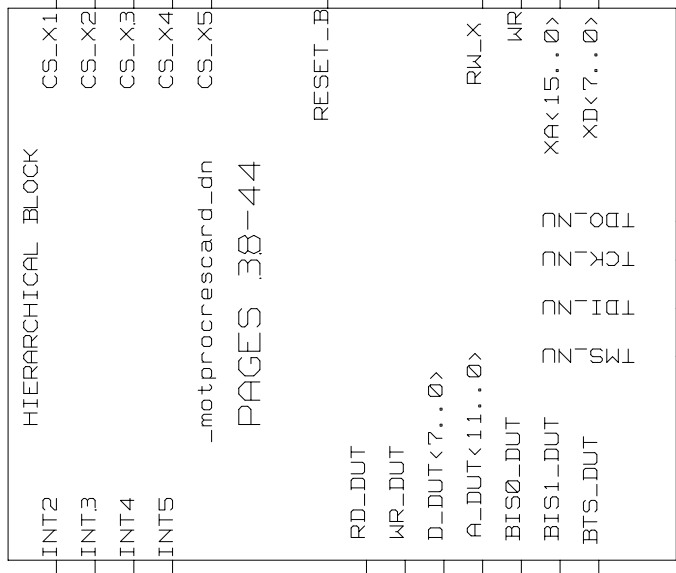
All signals inside a hierarchy block are local, with exception for V_{CC} and ground. In-port and out-port connectors are used to allow signals inside a hierarchy block to become accessible as pins on the hierarchy blocks symbol. From here, blocks are wired together as if they were ordinary components. The system diagram is shown again below, with schematic page numbers given for each functional block.

This system contained other hierarchy blocks that are not shown (primarily a single-port serial card and the DS33Z11 mainboard). Due to this, page numbers will not be continuous and some gaps in numbering will be seen when referring to the total page count. However, page numbers inside any given hierarchy block will be continuous.

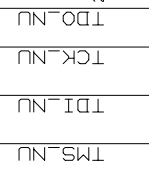




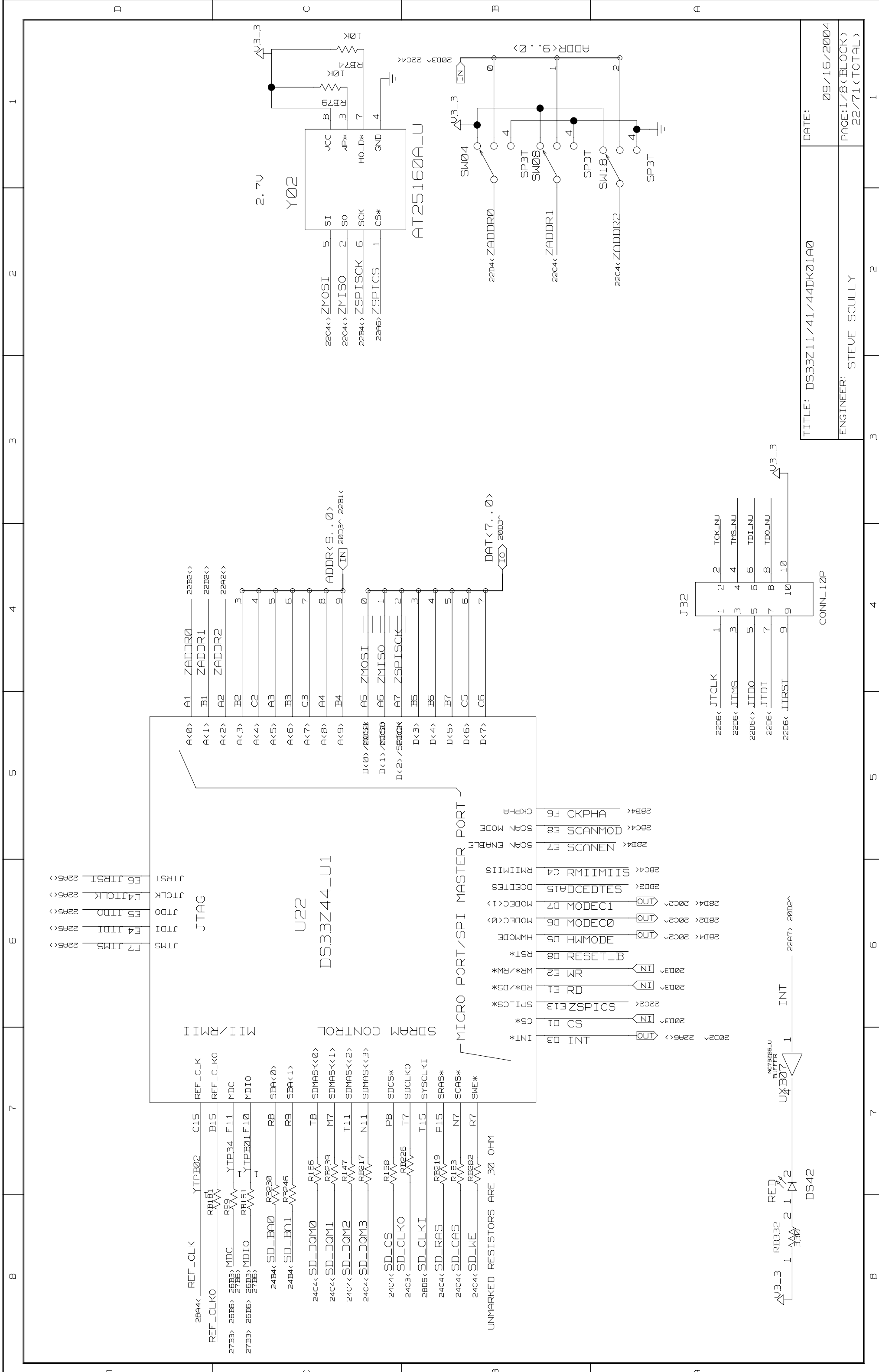
I 1



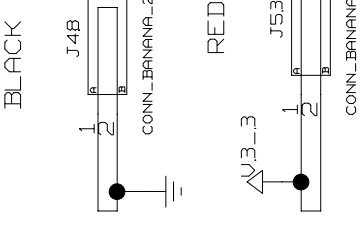
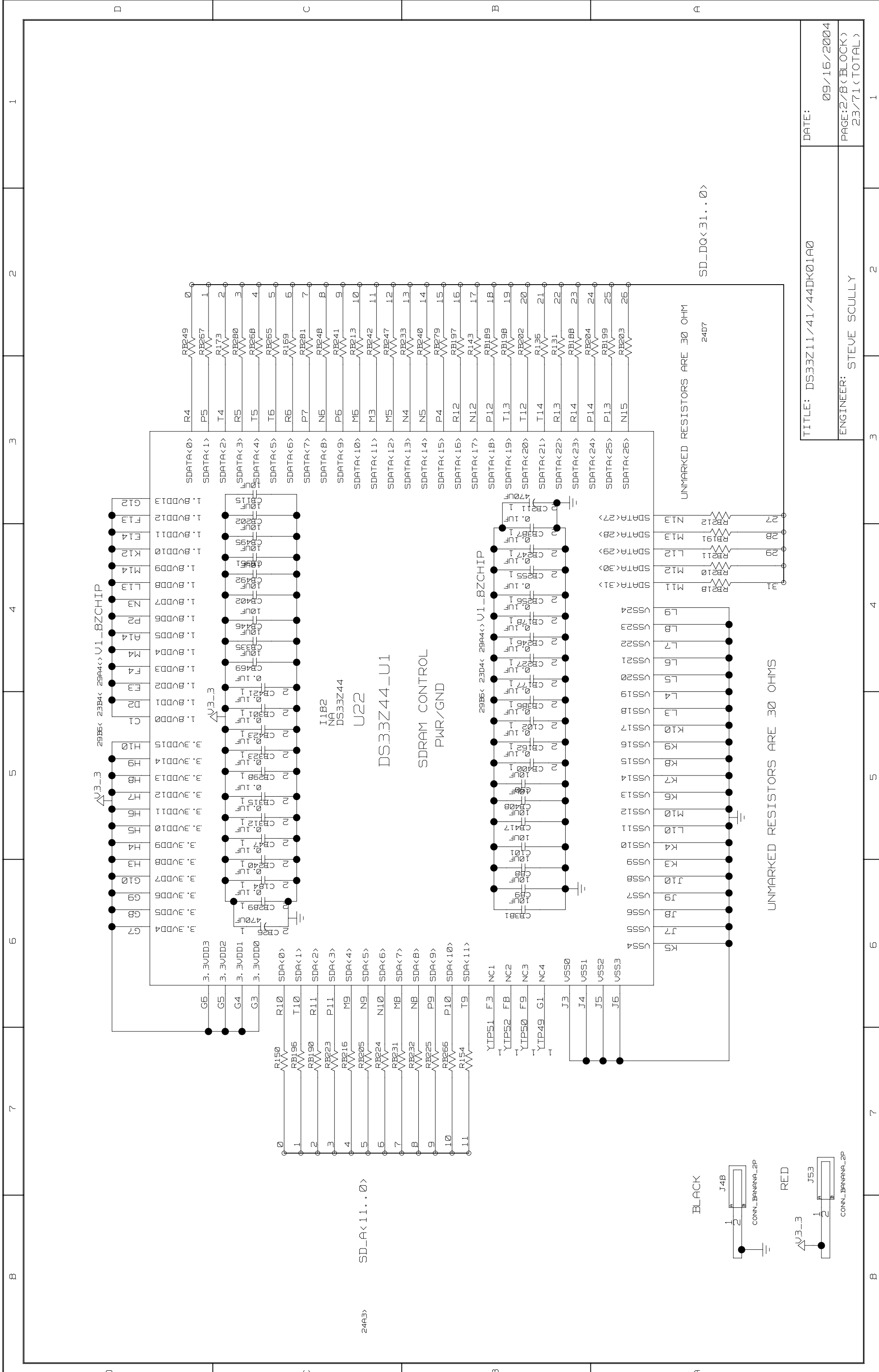
-motprorescard_dn
PAGES 38-44



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:2/2(BLOCK) 21/71(TOTAL)



TITLE: DS33Z11/41/44DK01A0
 DATE: 09/16/2004
 ENGINEER: STEVE SCULLY
 PAGE:1/8 (BLOCK)
 22/71 (TOTAL)



SD_A<11..0>
24A3>

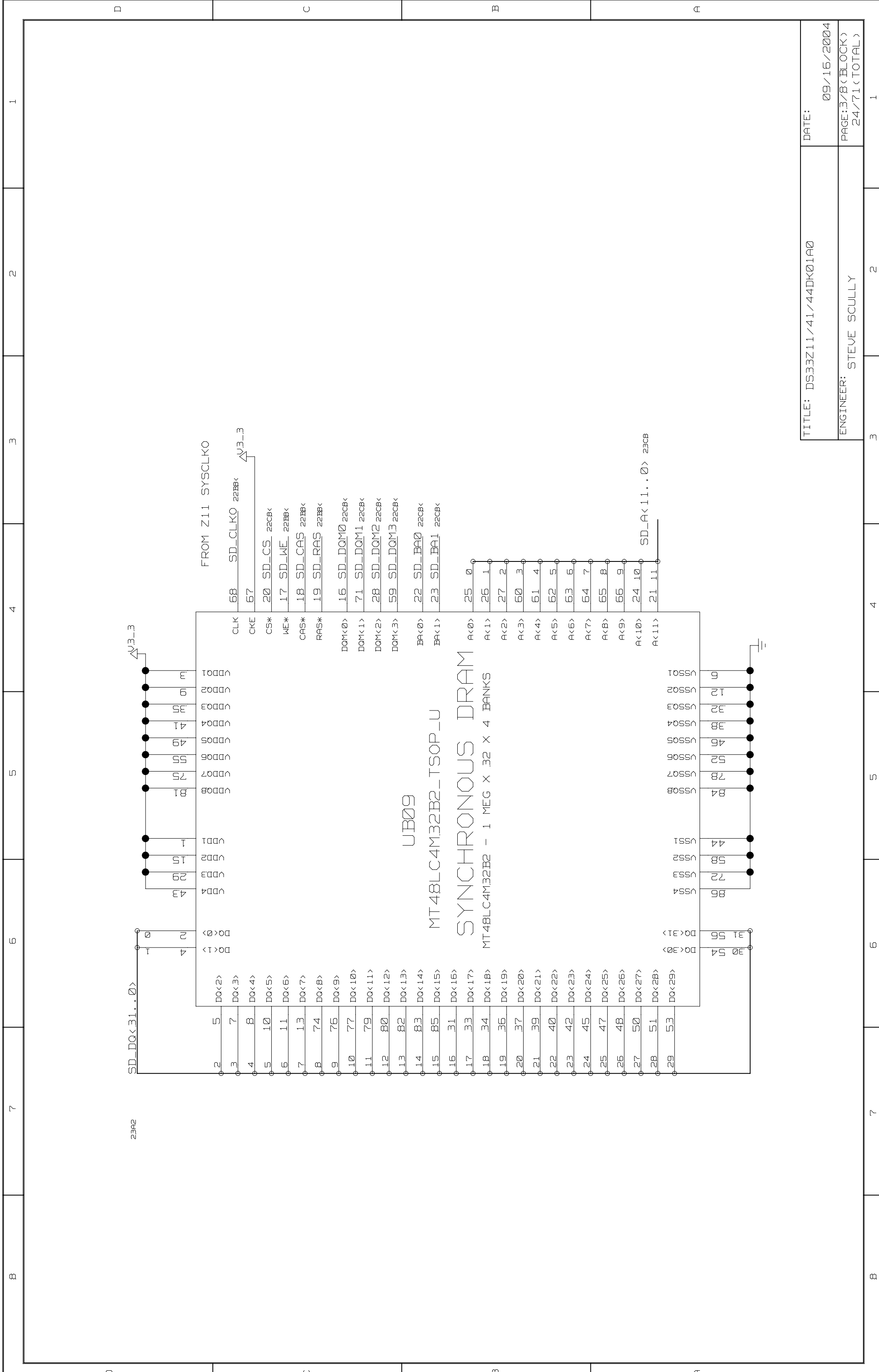
SD_DQ<31..0>

TITLE: DS33Z11/41/44DK01A0

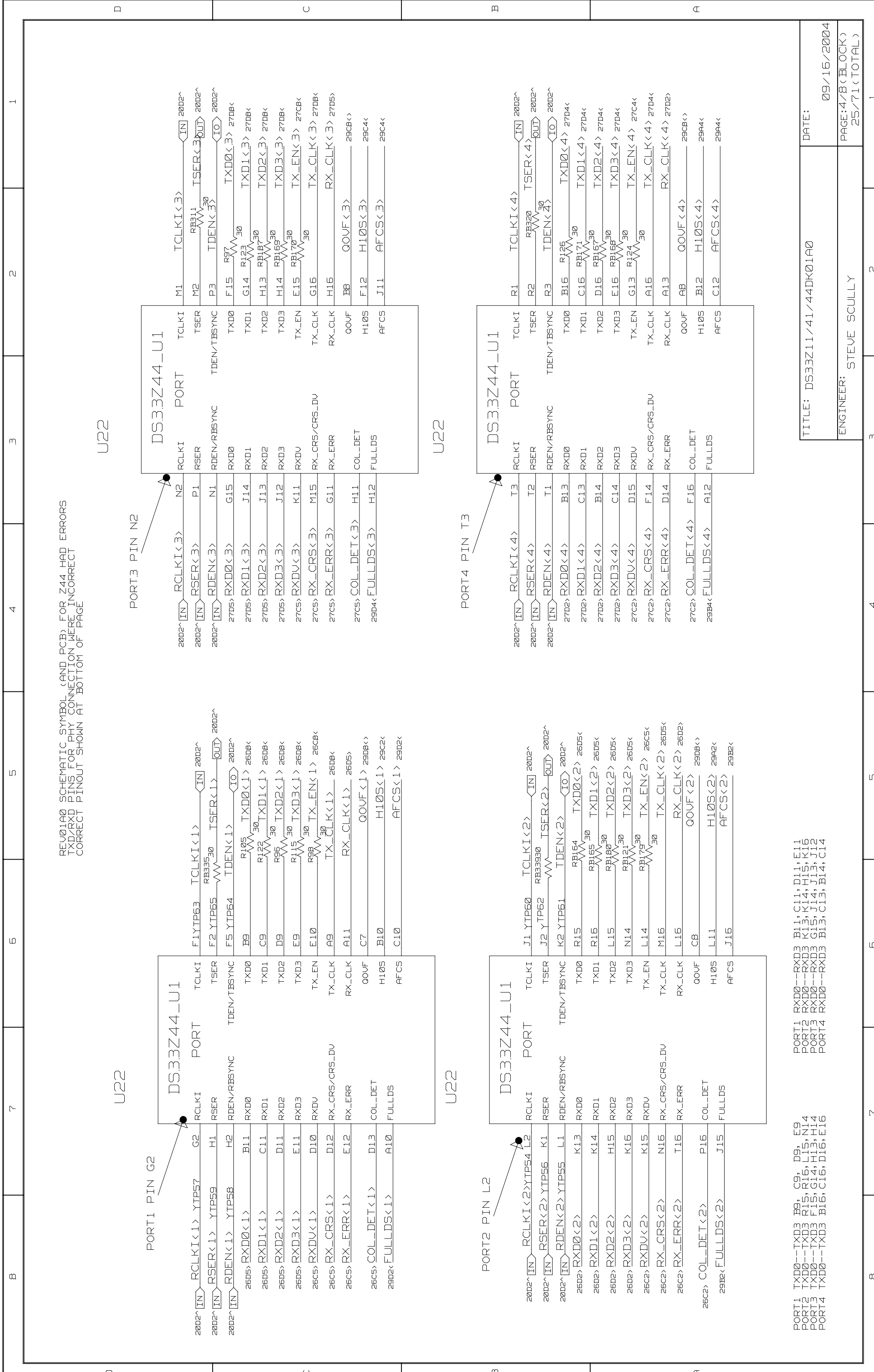
DATE: 09/16/2004

ENGINEER: STEVE SCULLY

PAGE:2/8 (BLOCK)
23/71 (TOTAL)



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:3/8(BLOCK) 24/71(TOTAL)



REV01A0 SCHEMATIC SYMBOL (AND PCB) FOR Z44 HAD ERRORS
TXD/RXD PINS FOR PHY CONNECTION WERE INCORRECT
CORRECT PINOUT SHOWN AT BOTTOM OF PAGE

U22

PORT1 PIN G2

PORT3 PIN N2

PORT2 PIN L2

PORT4 PIN T3

DS33Z44-U1

20D2< IN	RCLKI<1>	YTP57	G2	RCLKI	TCLKI
20D2< IN	RSER<1>	YTP59	H1	RSER	TSER
20D2< IN	RDEN<1>	YTP58	H2	RDEN/RBSYNC	TDEN/TBSYNC
26D5<	RXD0<1>	B11	B11	RXD0	TXD0
26D5<	RXD1<1>	C11	C11	RXD1	TXD1
26D5<	RXD2<1>	D11	D11	RXD2	TXD2
26D5<	RXD3<1>	E11	E11	RXD3	TXD3
26C5<	RXDV<1>	D10	D10	RXDV	TX_EN
26C5<	RX_CRS<1>	D12	D12	RX_CRS/CRS_DV	TX_CLK
26C5<	RX_ERR<1>	E12	E12	RX_ERR	RX_CLK
26C5<	COL_DET<1>	D13	D13	COL_DET	QOVF
29D2<	FULLDS<1>	A10	A10	FULLDS	H10S
					AFCS

DS33Z44-U1

20D2< IN	RCLKI<3>	N2	RCLKI	TCLKI
20D2< IN	RSER<3>	P1	RSER	TSER
20D2< IN	RDEN<3>	N1	RDEN/RBSYNC	TDEN/TBSYNC
27D5<	RXD0<3>	G15	RXD0	TXD0
27D5<	RXD1<3>	J14	RXD1	TXD1
27D5<	RXD2<3>	J13	RXD2	TXD2
27D5<	RXD3<3>	J12	RXD3	TXD3
27C5<	RXDV<3>	K11	RXDV	TX_EN
27C5<	RX_CRS<3>	M15	RX_CRS/CRS_DV	TX_CLK
27C5<	RX_ERR<3>	G11	RX_ERR	RX_CLK
27C5<	COL_DET<3>	H11	COL_DET	QOVF
29D4<	FULLDS<3>	H12	FULLDS	H10S
				AFCS

DS33Z44-U1

20D2< IN	RCLKI<2>	YTP54	L2	RCLKI	TCLKI
20D2< IN	RSER<2>	YTP56	K1	RSER	TSER
20D2< IN	RDEN<2>	YTP55	L1	RDEN/RBSYNC	TDEN/TBSYNC
26D2<	RXD0<2>	K13	K13	RXD0	TXD0
26D2<	RXD1<2>	K14	K14	RXD1	TXD1
26D2<	RXD2<2>	H15	H15	RXD2	TXD2
26D2<	RXD3<2>	K16	K16	RXD3	TXD3
26C2<	RXDV<2>	K15	K15	RXDV	TX_EN
26C2<	RX_CRS<2>	N16	N16	RX_CRS/CRS_DV	TX_CLK
26C2<	RX_ERR<2>	T16	T16	RX_ERR	RX_CLK
26C2<	COL_DET<2>	P16	P16	COL_DET	QOVF
29B2<	FULLDS<2>	J15	J15	FULLDS	H10S
					AFCS

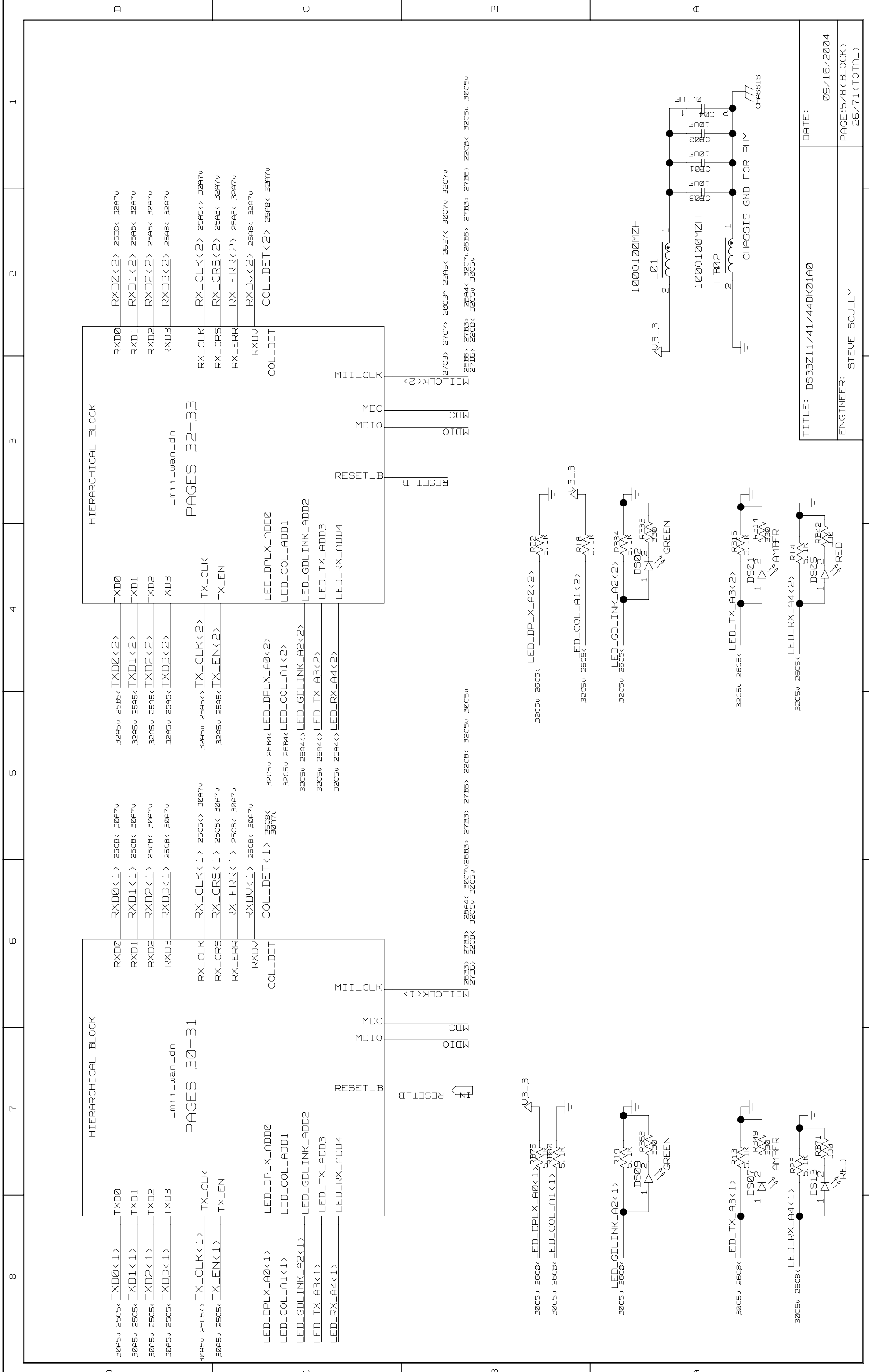
DS33Z44-U1

20D2< IN	RCLKI<4>	T3	RCLKI	TCLKI
20D2< IN	RSER<4>	T2	RSER	TSER
20D2< IN	RDEN<4>	T1	RDEN/RBSYNC	TDEN/TBSYNC
27D2<	RXD0<4>	B13	RXD0	TXD0
27D2<	RXD1<4>	C13	RXD1	TXD1
27D2<	RXD2<4>	B14	RXD2	TXD2
27D2<	RXD3<4>	C14	RXD3	TXD3
27C2<	RXDV<4>	D15	RXDV	TX_EN
27C2<	RX_CRS<4>	F14	RX_CRS/CRS_DV	TX_CLK
27C2<	RX_ERR<4>	D14	RX_ERR	RX_CLK
27C2<	COL_DET<4>	F16	COL_DET	QOVF
29B4<	FULLDS<4>	A12	FULLDS	H10S
				AFCS

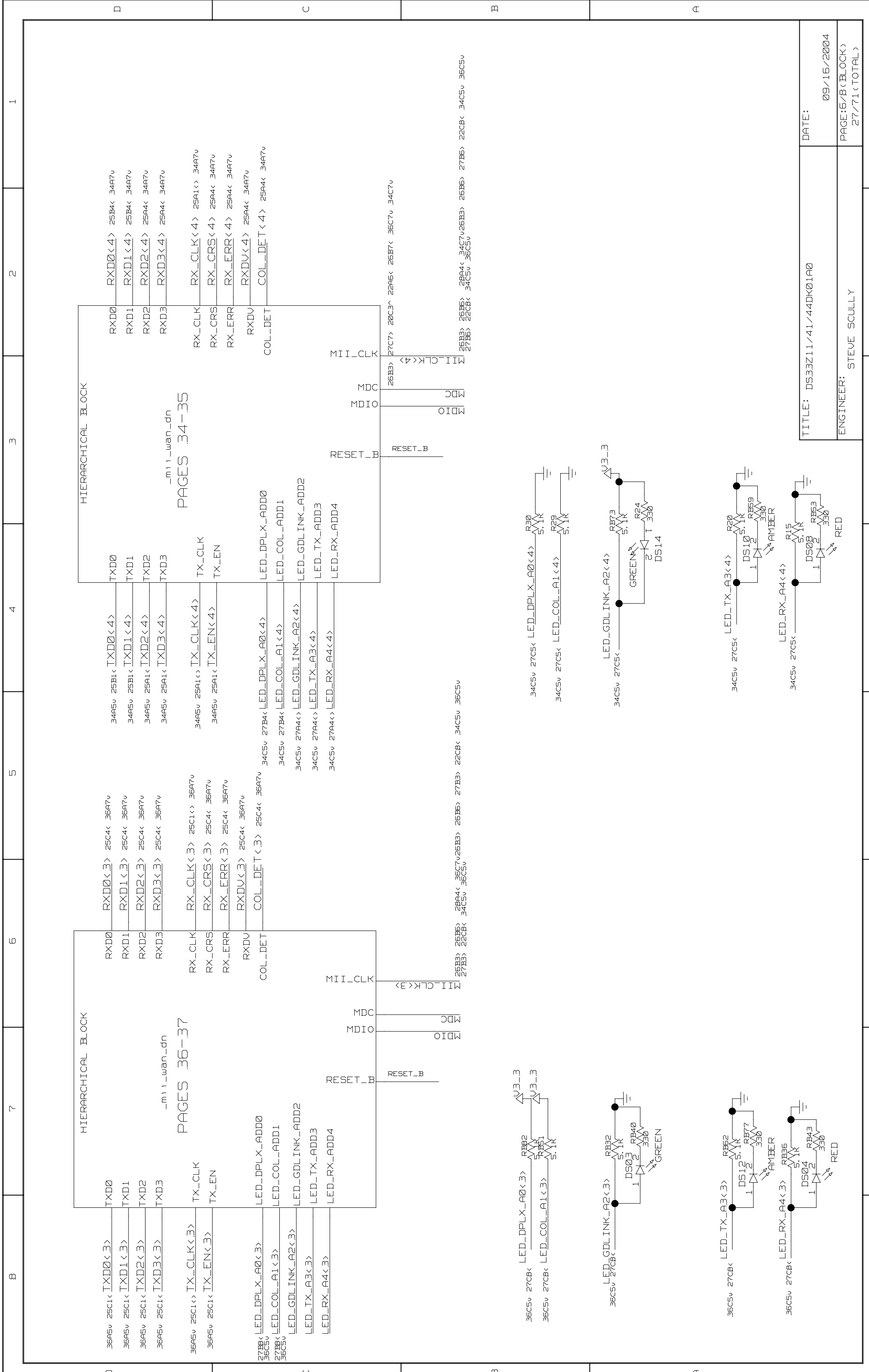
PORT1 TXD0--TXD3 B9, C9, D9, E9
PORT2 RXD0--RXD3 R15, R16, L15, N14
PORT3 TXD0--TXD3 F15, G14, H13, H14
PORT4 TXD0--TXD3 B16, C16, D16, E16

PORT1 RXD0--RXD3 B11, C11, D11, E11
PORT2 RXD0--RXD3 K13, K14, H15, K16
PORT3 RXD0--RXD3 G15, J14, J13, J12
PORT4 RXD0--RXD3 B13, C13, B14, C14

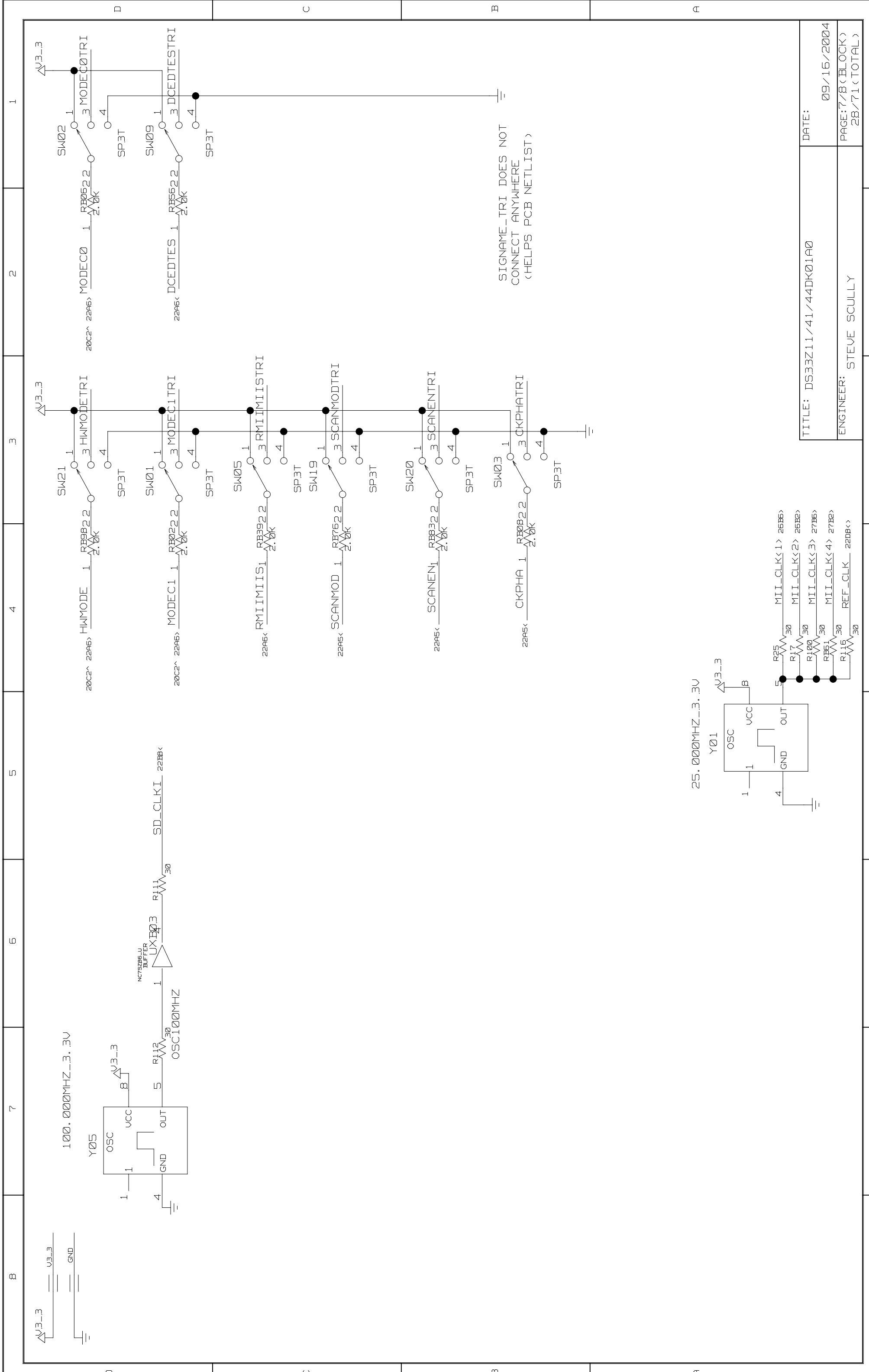
TITLE: DS33Z11/41/44DK01A0
ENGINEER: STEVE SCULLY
DATE: 09/16/2004
PAGE: 4/8 (BLOCK)
25/71 (TOTAL)



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 15/8 (BLOCK) 25/71 (TOTAL)

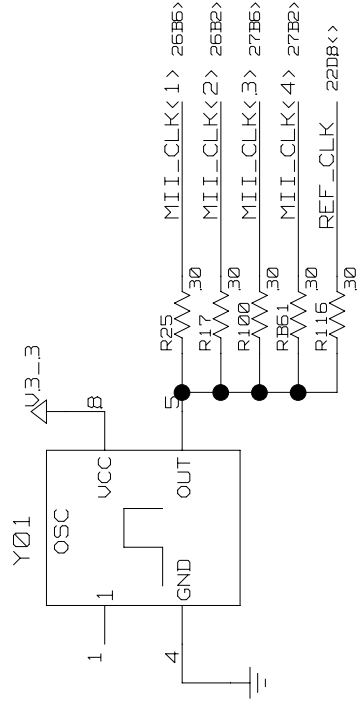


TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 16/8 (BLOCK) 27/71 (TOTAL)

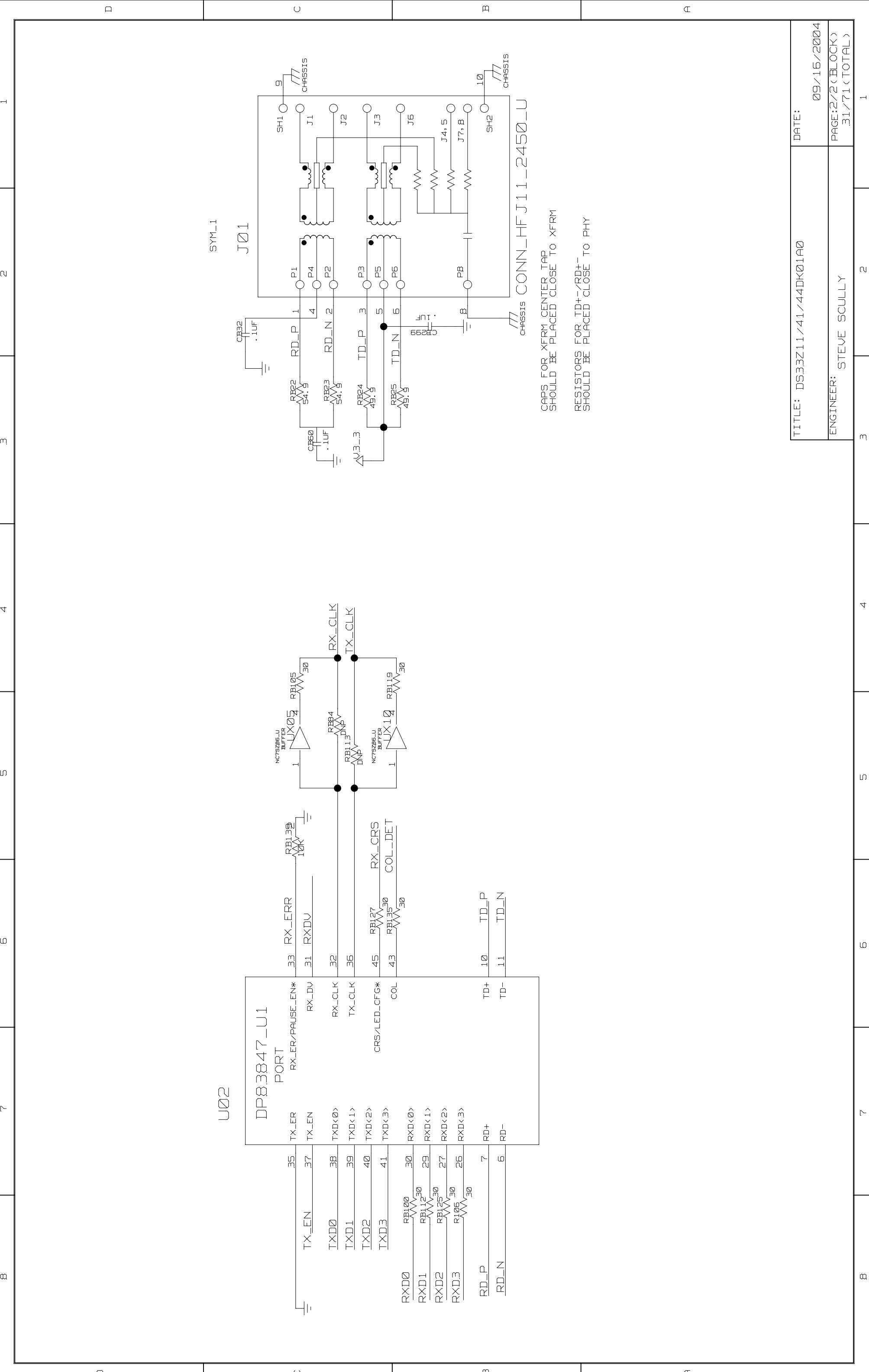


SIGNAME_TRI DOES NOT CONNECT ANYWHERE (HELPS PCB NETLIST)

25.000MHZ-.3V

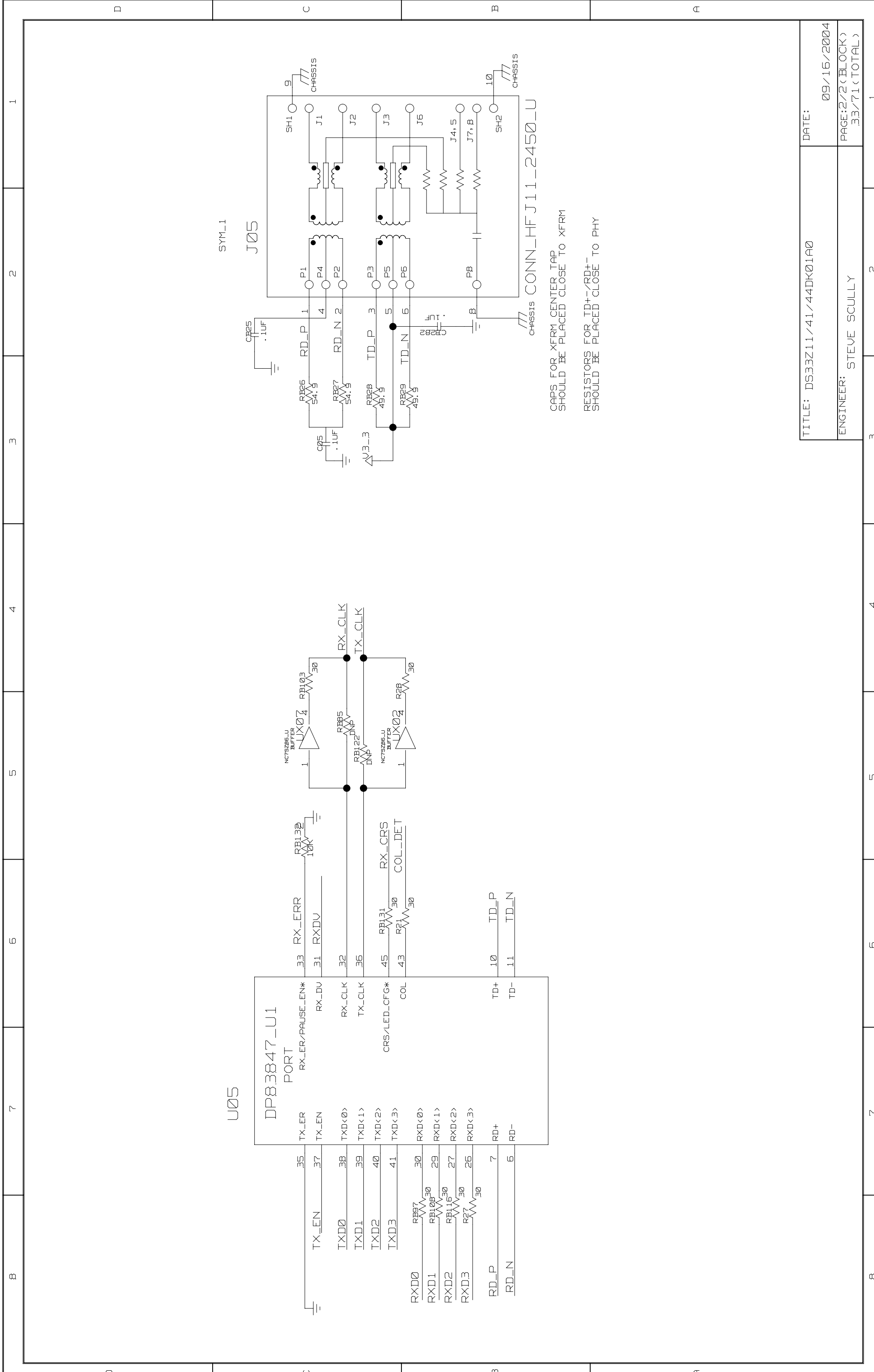


TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 7/8 (BLOCK) 28/71 (TOTAL)



CAPS FOR XFRM CENTER TAP SHOULD BE PLACED CLOSE TO XFRM
RESISTORS FOR TD+/-/RD+/- SHOULD BE PLACED CLOSE TO PHY

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:2/2(BLOCK) .31/71(TOTAL)



U05

SYM_1

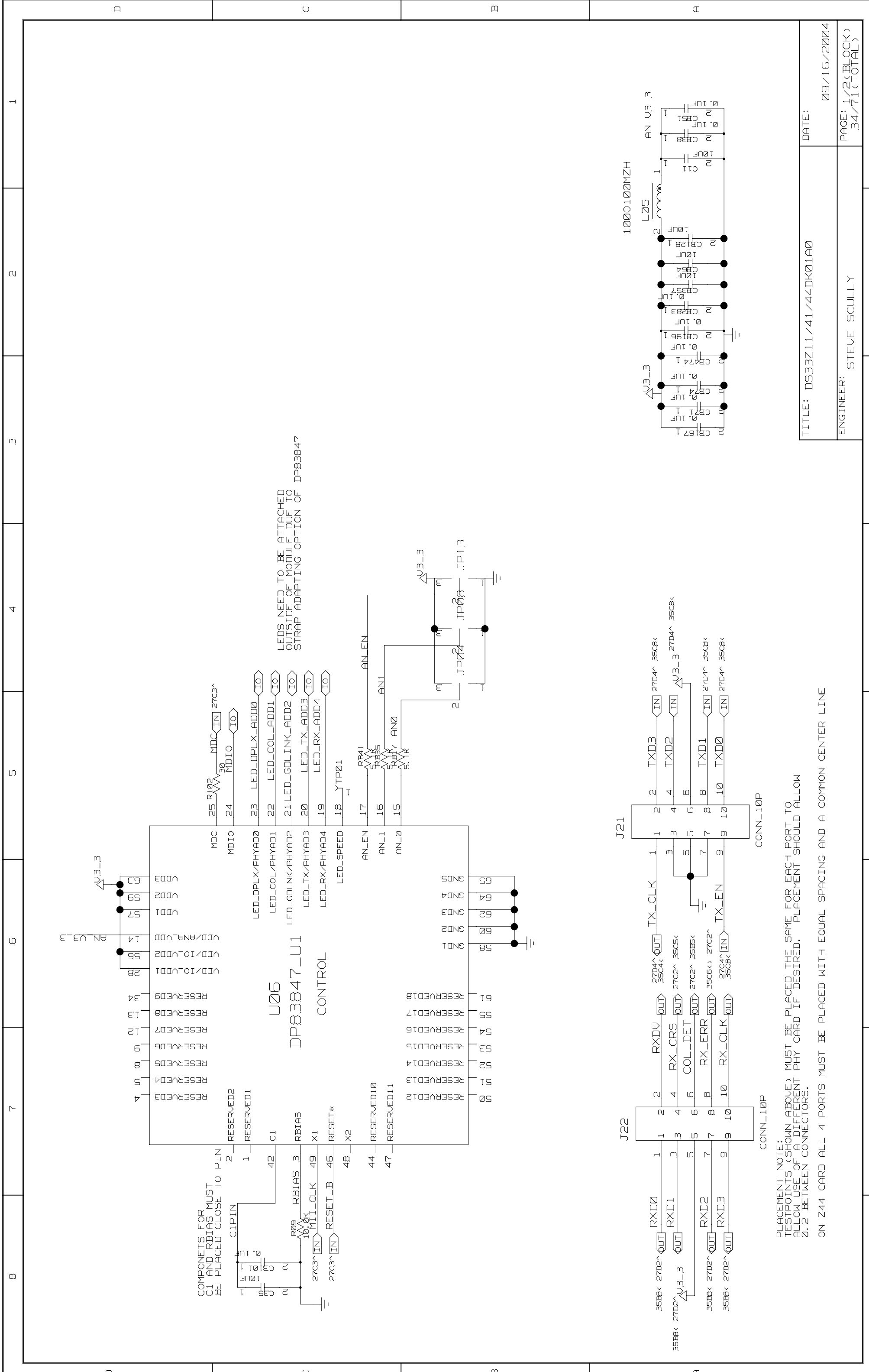
DP8.3847-U1	
35 TX_EN	33 RX_ERR
37 TX_EN	31 RXDV
38 TXD<0>	32 RX_CLK
39 TXD<1>	36 TX_CLK
40 TXD<2>	45 RX_CRD
41 TXD<3>	43 TX_CRD
30 RXD<0>	30 COL_DET
29 RXD<1>	30 COL
27 RXD<2>	
26 RXD<3>	
7 RD+	10 TD_P
6 RD-	11 TD_N

CAPS FOR XFRM CENTER TAP SHOULD BE PLACED CLOSE TO XFRM

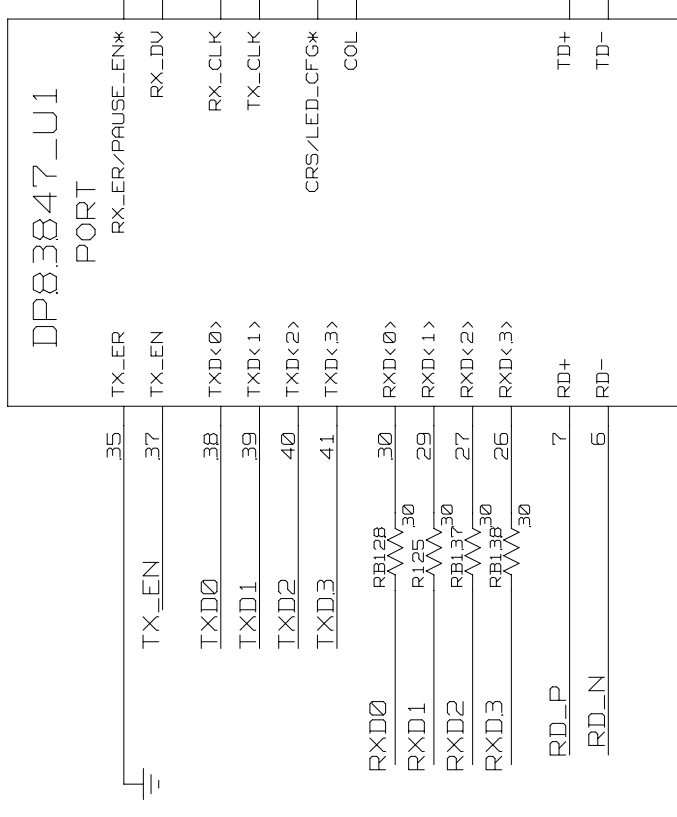
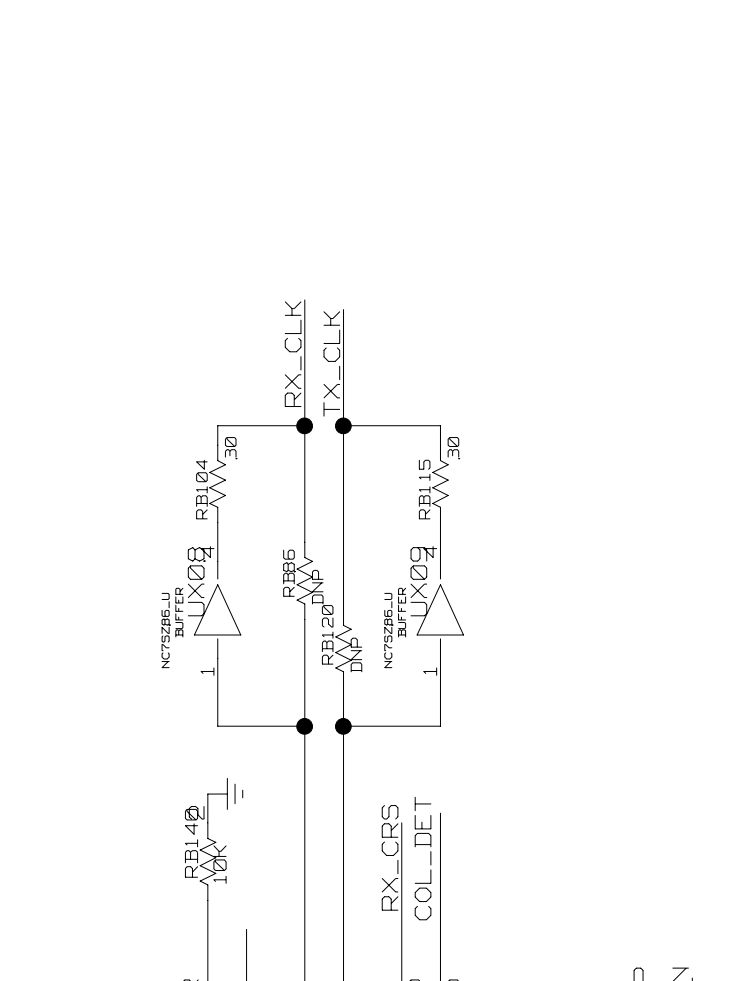
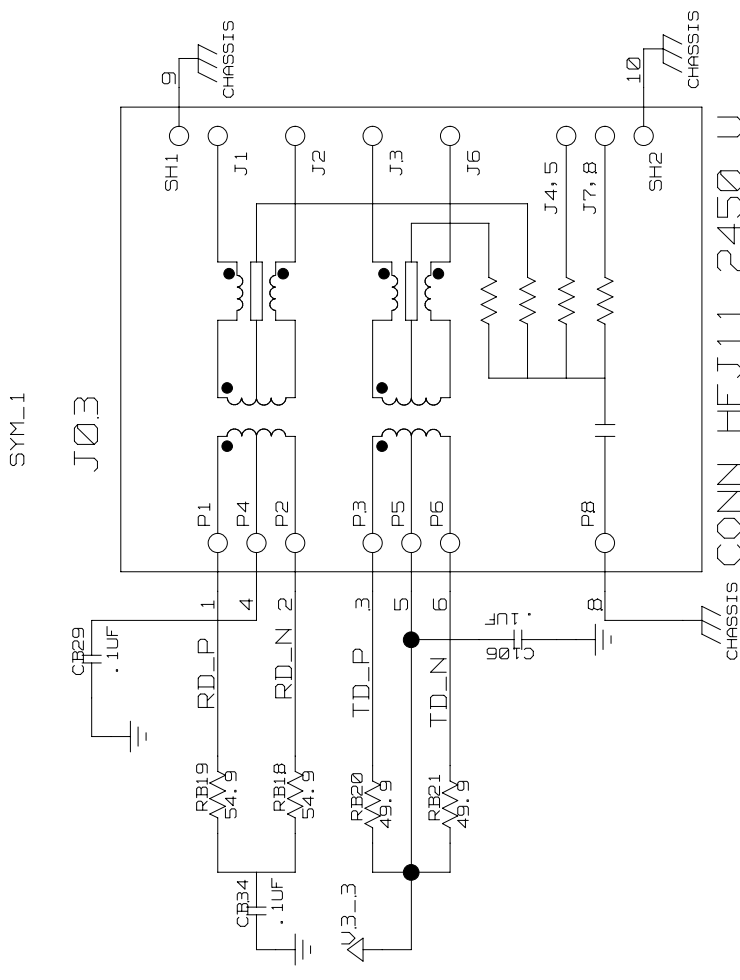
RESISTORS FOR TD+/-/RD+/- SHOULD BE PLACED CLOSE TO PHY

CONN_HF J11-2450-U

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:2/2 (BLOCK) .33/71 (TOTAL)



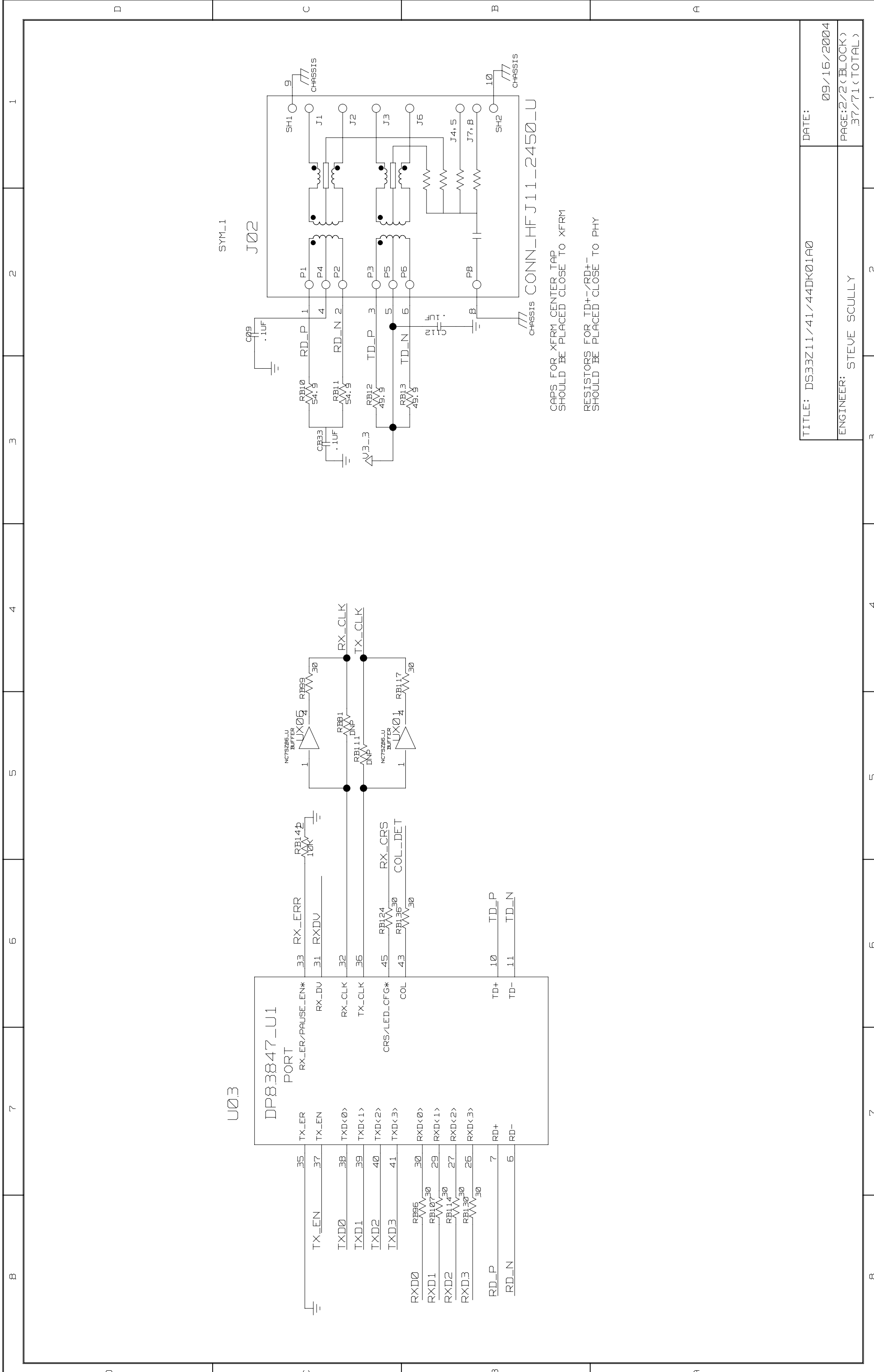
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 1/2 (BLOCK) 34/71 (TOTAL)



CAPS FOR XFRM CENTER TAP SHOULD BE PLACED CLOSE TO XFRM

RESISTORS FOR IDH+/RD+ SHOULD BE PLACED CLOSE TO PHY

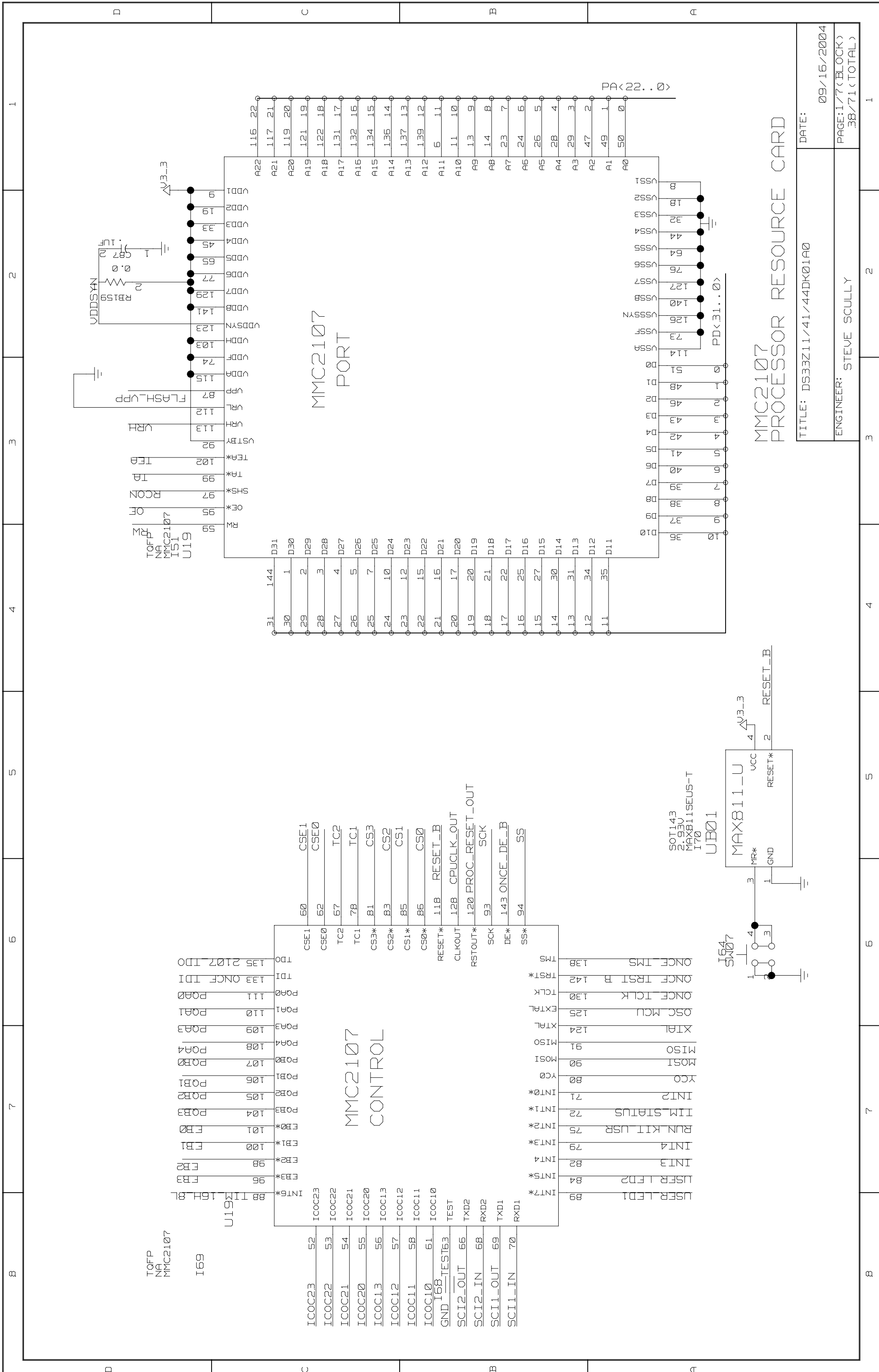
TITLE:	DS33Z11/41/44DK01A0	DATE:	09/16/2004
ENGINEER:	STEVE SCULLY	PAGE:	2/2 (BLOCK)
		TOTAL:	35/71 (TOTAL)



CAPS FOR XFRM CENTER TAP SHOULD BE PLACED CLOSE TO XFRM

RESISTORS FOR TD+/-/RD+/- SHOULD BE PLACED CLOSE TO PHY

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:2/2 (BLOCK) .37/71 (TOTAL)



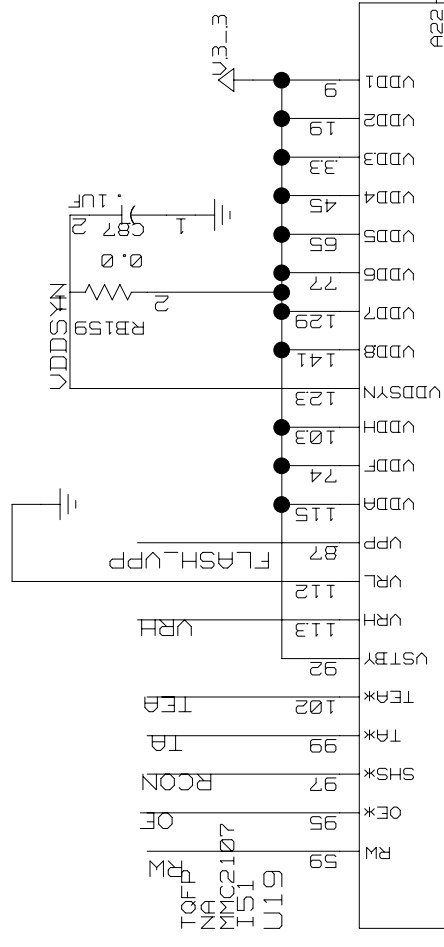
TQFP
NA
MMC2107

I69

MMC2107 CONTROL

ICOC23	52	ICOC23	INT*	88	TIK	16H	8L
ICOC22	53	ICOC22	INT*	89	FBI*	FBI	96
ICOC21	54	ICOC21	INT*	90	FBI*	FBI	98
ICOC20	55	ICOC20	INT*	91	FBI*	FBI	100
ICOC13	56	ICOC13	INT*	92	FBI*	FBI	101
ICOC12	57	ICOC12	INT*	93	FB2	FB2	104
ICOC11	58	ICOC11	INT*	94	FB3	FB3	105
ICOC10	61	ICOC10	INT*	95	FB1*	FB1*	106
GND 168	TEST63	TEST	INT*	96	FB2	FB2	107
SCI2_OUT 66	TXD2	TXD2	INT*	97	FB3	FB3	108
SCI2_IN 68	RXD2	RXD2	INT*	98	FB1*	FB1*	109
SCI1_OUT 69	TXD1	TXD1	INT*	99	FB2	FB2	110
SCI1_IN 70	RXD1	RXD1	INT*	100	FB3	FB3	111
			INT*	101	FB1*	FB1*	112
			INT*	102	FB2*	FB2*	113
			INT*	103	FB3*	FB3*	114
			INT*	104	FB1*	FB1*	115
			INT*	105	FB2*	FB2*	116
			INT*	106	FB3*	FB3*	117
			INT*	107	FB1*	FB1*	118
			INT*	108	FB2*	FB2*	119
			INT*	109	FB3*	FB3*	120
			INT*	110	FB1*	FB1*	121
			INT*	111	FB2*	FB2*	122
			INT*	112	FB3*	FB3*	123
			INT*	113	FB1*	FB1*	124
			INT*	114	FB2*	FB2*	125
			INT*	115	FB3*	FB3*	126
			INT*	116	FB1*	FB1*	127
			INT*	117	FB2*	FB2*	128
			INT*	118	FB3*	FB3*	129
			INT*	119	FB1*	FB1*	130
			INT*	120	FB2*	FB2*	131
			INT*	121	FB3*	FB3*	132
			INT*	122	FB1*	FB1*	133
			INT*	123	FB2*	FB2*	134
			INT*	124	FB3*	FB3*	135
			INT*	125	FB1*	FB1*	136
			INT*	126	FB2*	FB2*	137
			INT*	127	FB3*	FB3*	138
			INT*	128	FB1*	FB1*	139
			INT*	129	FB2*	FB2*	140
			INT*	130	FB3*	FB3*	141
			INT*	131	FB1*	FB1*	142
			INT*	132	FB2*	FB2*	143
			INT*	133	FB3*	FB3*	144

MMC2107 PORT

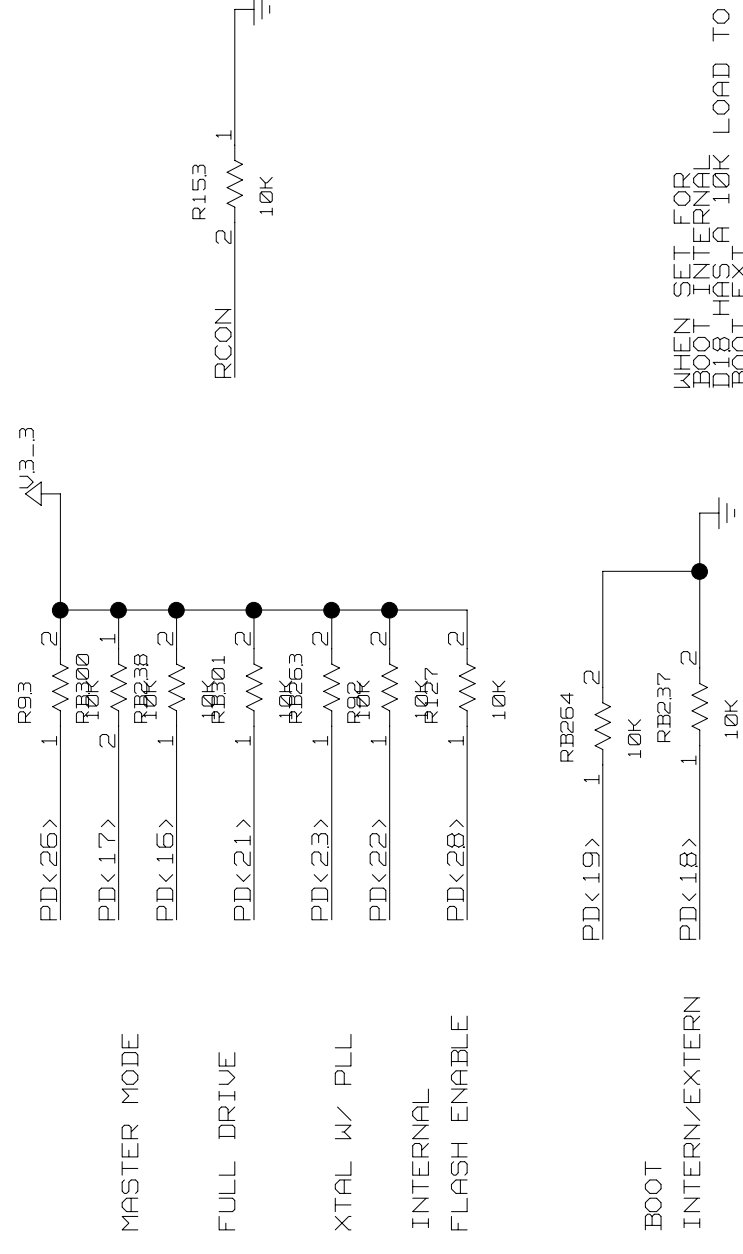


MMC2107 PROCESSOR RESOURCE CARD

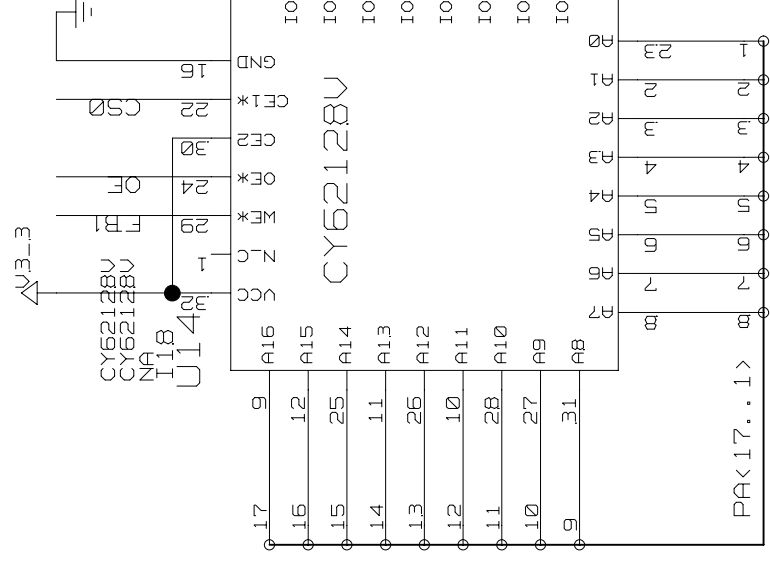
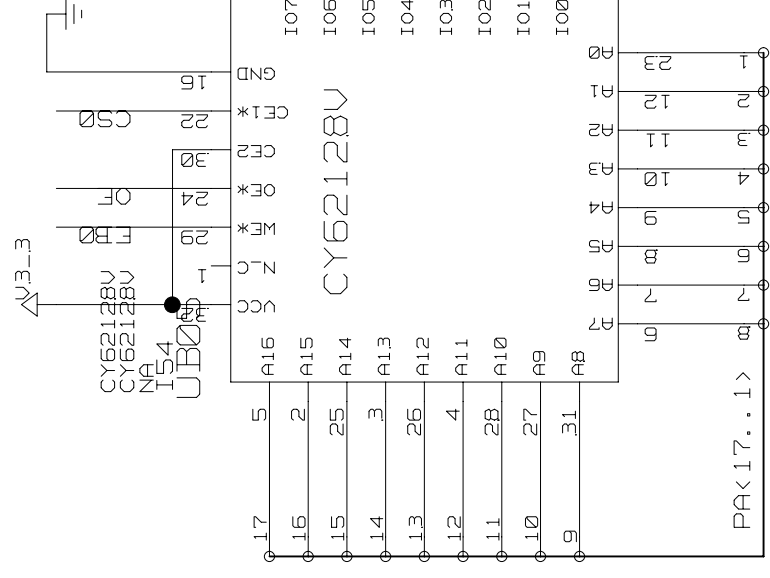
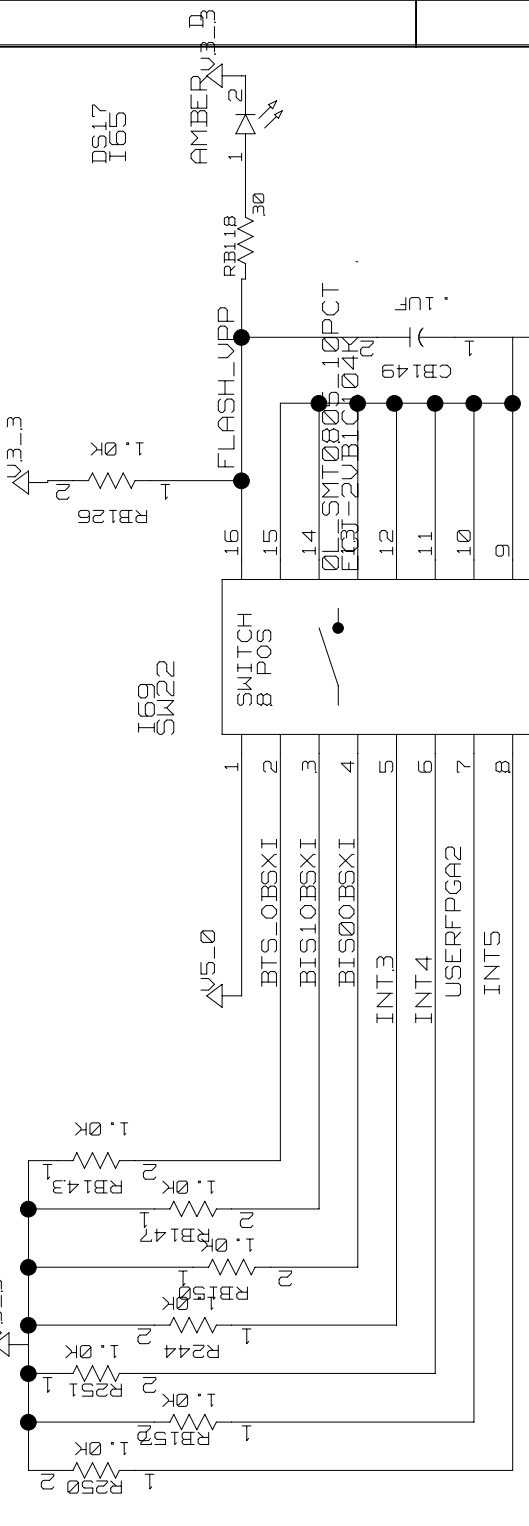
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 1/7 (BLOCK) .38/71 (TOTAL)



RESET CONFIGURATION



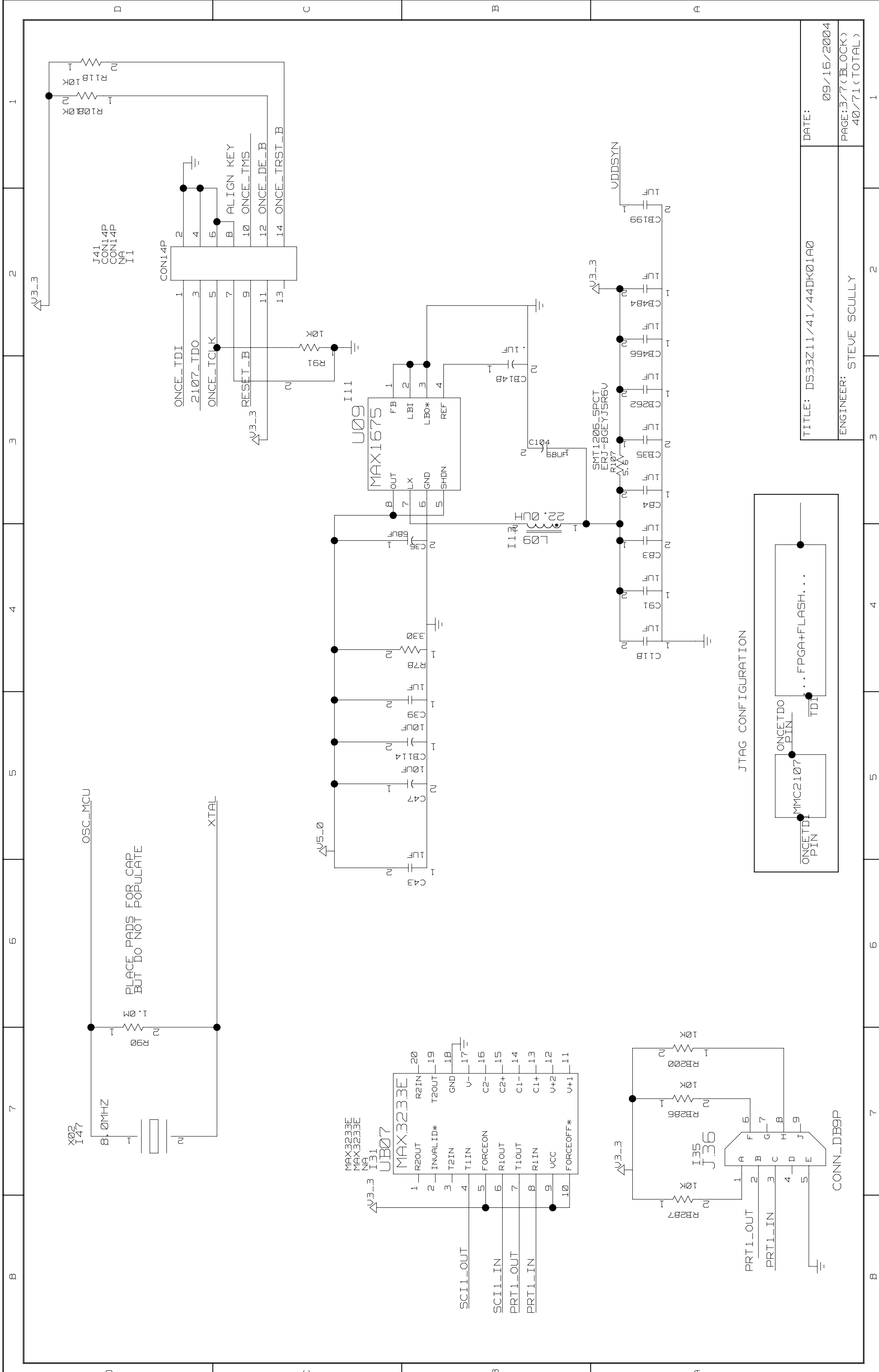
WHEN SET FOR
BOOT INTERNAL
DIB HAS A 10K LOAD TO GND
BOOT EXTERNAL
DIB HAS A 10.5K LOAD TO V3V



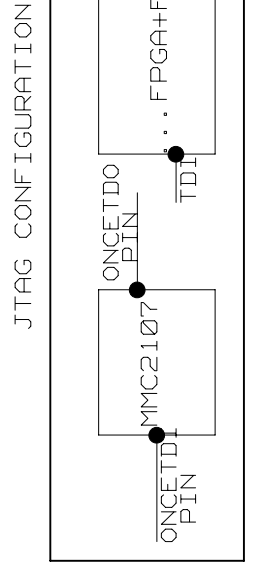
RESET AND CHIP CONFIGURATION

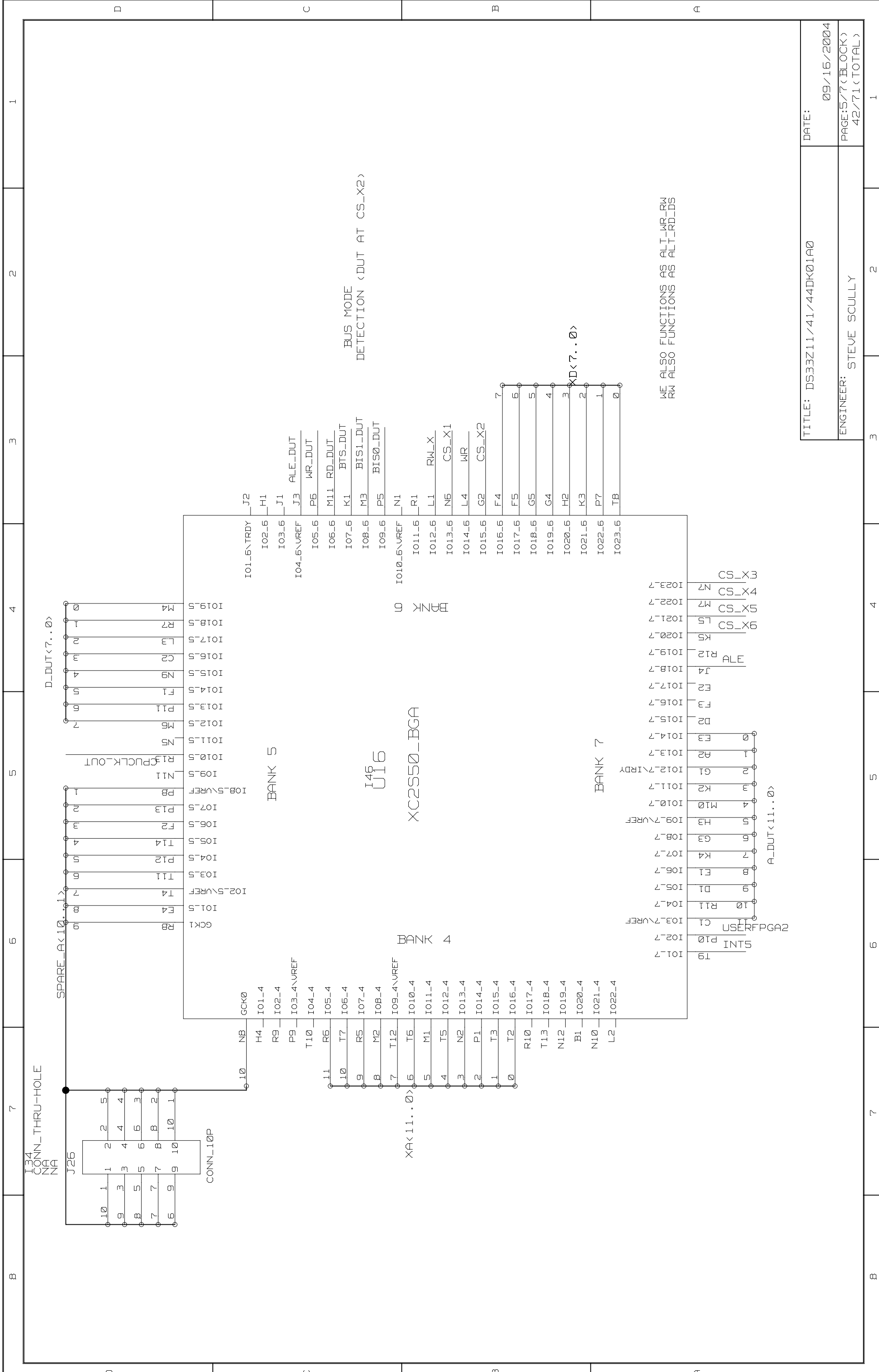
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/7 (BLOCK) .39/71 (TOTAL)

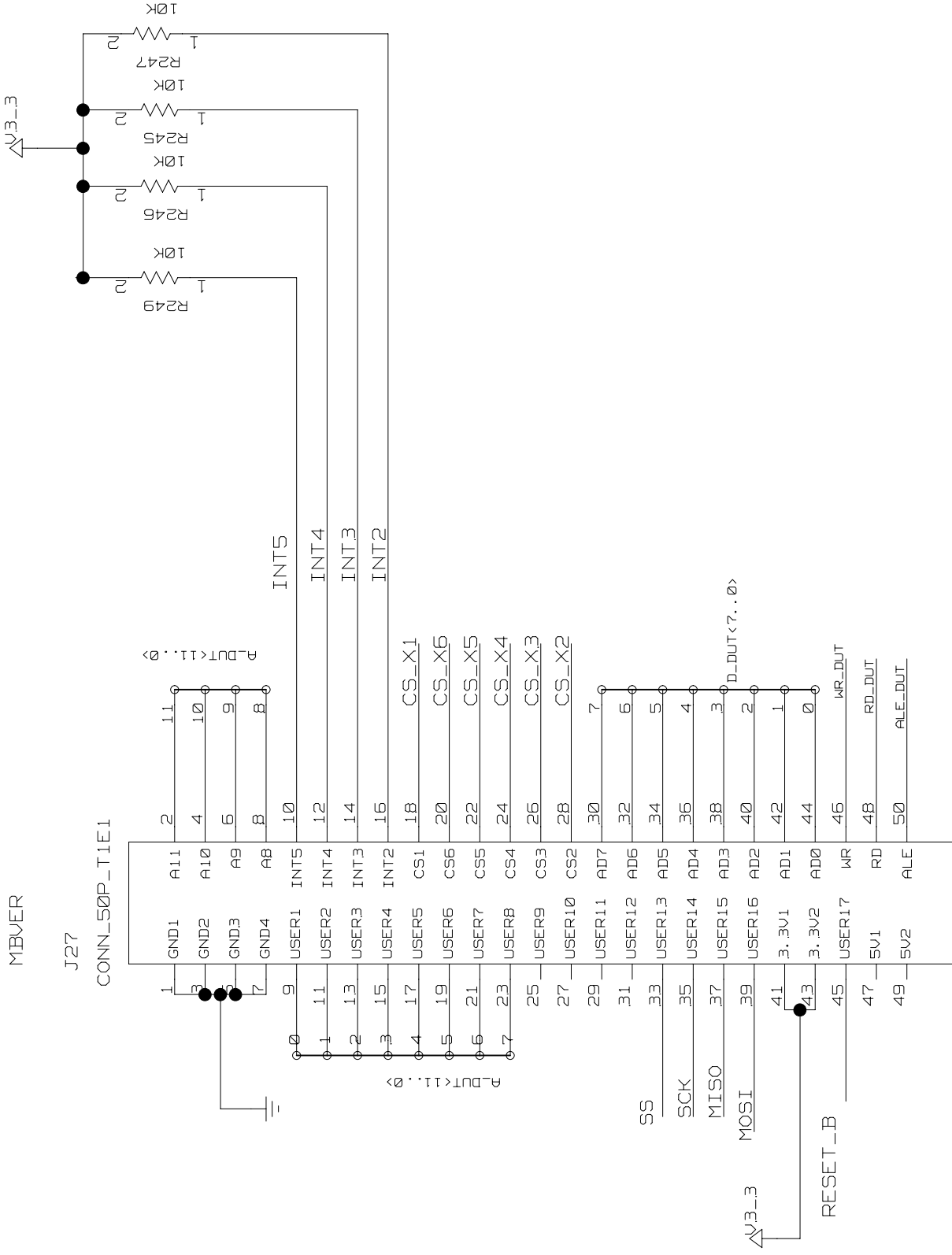
CR-40 : e:\ztopd\lib\ztopdn\ztopdn\ztop_1\lib\ztop_1\motprorescard_dn\sch_1\page3



TITLE: DS33Z11/41/44DK01A0
 ENGINEER: STEVE SCULLY
 DATE: 09/16/2004
 PAGE:377(BLOCK)
 40/71(TOTAL)





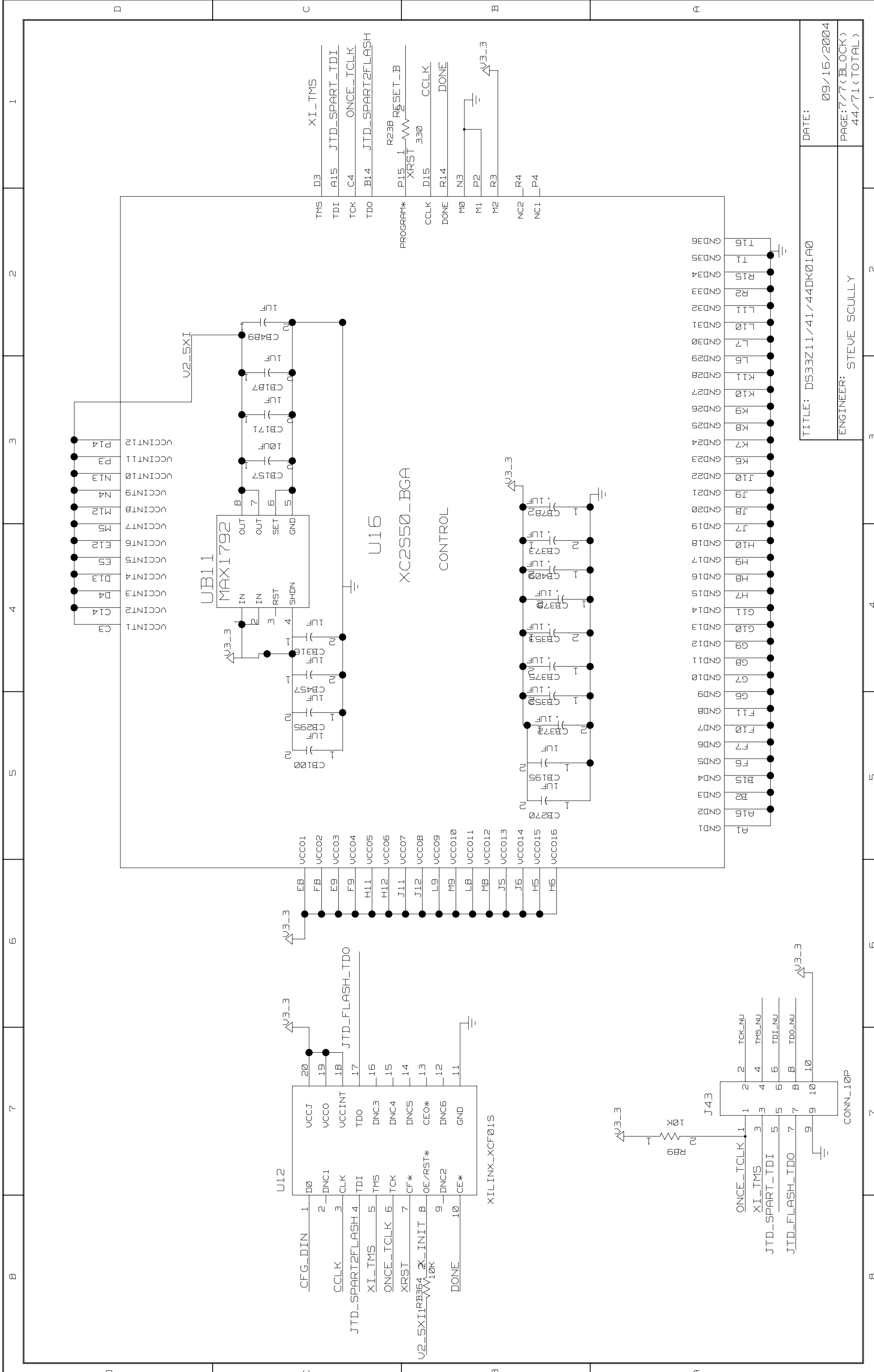


MBVER

J27

CONN_50P_T1E1

D	C	B	A
	<p>INT5 39C3<> 42A6<> 43C6<> 21C7<^</p> <p>INT4 39A7<> 39C3<> 43C6<> 21C7<^</p> <p>INT3 39A7<> 39D3<> 43C6<> 21C7<^</p> <p>INT2 39A7<> 43C6<> 21C7<^</p>	<p>RESET_B [OUT] 38A4< 38BE<> 40C3<> 21C5< 43A7< 44B1<</p> <p>BTS_DUT [IN] 42C3<> 21B7<^</p> <p>BIS0_DUT [IN] 42C3<> 21B7<^</p> <p>BIS1_DUT [IN] 42C3<> 21B7<^</p> <p>TDO_NU [OUT] 44A6<> 21B6<^</p> <p>TCK_NU [IN] 44A6<> 21B6<^</p> <p>TDI_NU [IN] 44A6<> 21B6<^</p> <p>TMS_NU [IN] 44A6<> 21B6<^</p> <p>CS_X4 [OUT] 42A4<> 43B6<> 21C5<^</p> <p>CS_X5 [OUT] 42A4<> 43B6<> 21C5<^</p> <p>CS_X1 [OUT] 42B3<> 43B6<> 21C5<^</p> <p>CS_X2 [OUT] 42B3<> 43B6<> 21C5<^</p> <p>CS_X3 [OUT] 42A4<> 43B6<> 21C5<^</p> <p>NR_X [OUT] 42B3<> 21B5<^</p> <p>WR_DUT [OUT] 42B3<> 21B5<^</p> <p>RD_DUT [OUT] 42C3<> 43A6<> 21B7<^</p> <p>RD_DUT [OUT] 42C3<> 43A6<> 21B7<^</p> <p>A_DUT<11..0></p> <p>D_DUT<7..0></p> <p>XD<7..0></p>	<p>42B7 21B5<^XA<15..0></p> <p>D_DUT<7..0></p> <p>XD<7..0></p>
			<p>TITLE: DS33Z11/41/44DK01A0</p> <p>ENGINEER: STEVE SCULLY</p> <p>DATE: 09/16/2004</p> <p>PAGE:6/7 (BLOCK)</p> <p>43/71 (TOTAL)</p>



D3	XI_TMS
A15	JTD_SPART_TDI
C4	ONCE_TCLK
B14	JTD_SPART2FLASH
P15	R23B RESET_B
XRST	330
D15	CCLK
R14	DONE
M0	
M1	
M2	V3-3
NC2	R4
NC1	P4

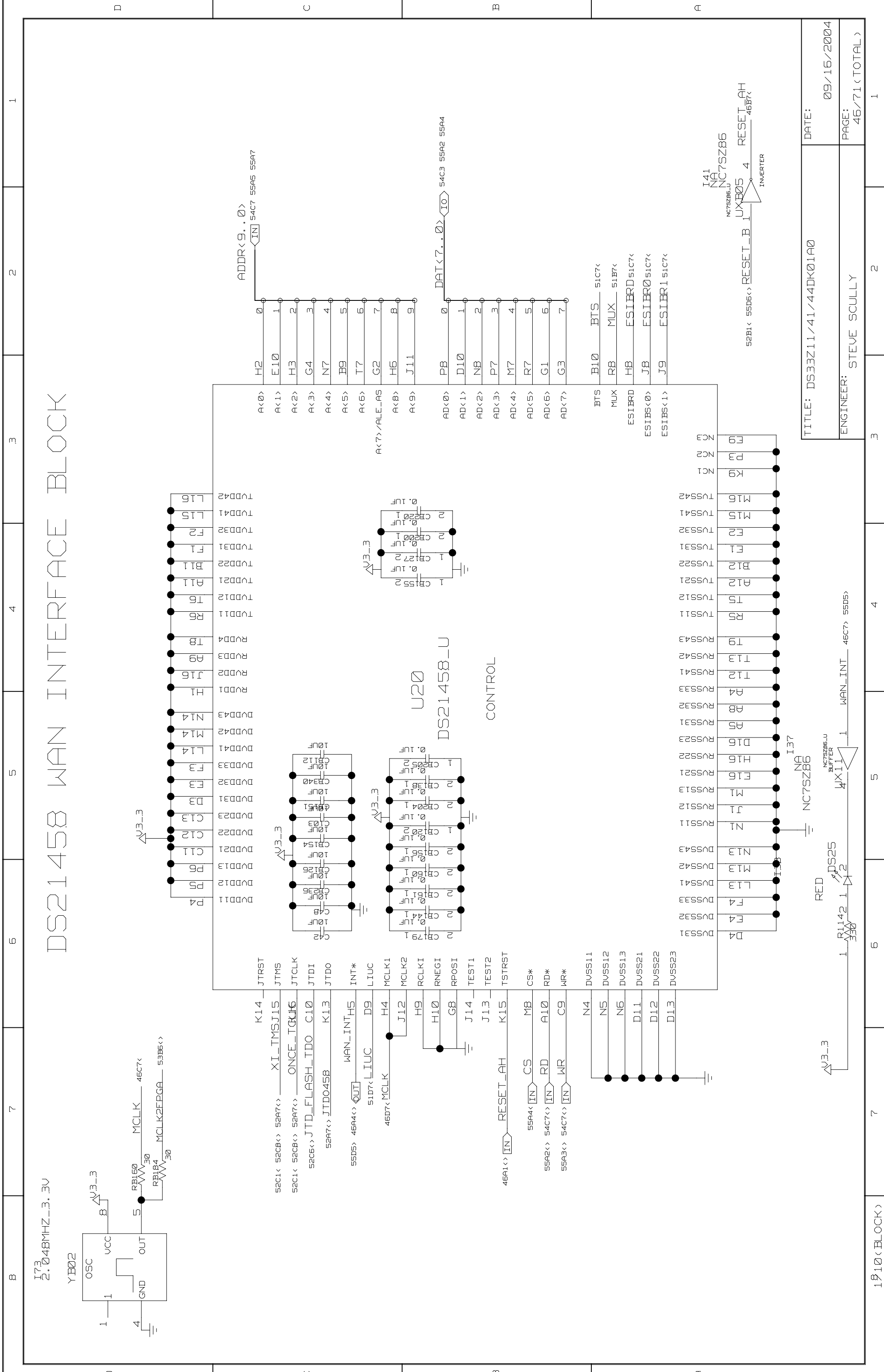
EB	VCC01
FB	VCC02
E9	VCC03
F9	VCC04
H11	VCC05
H12	VCC06
J11	VCC07
J12	VCC08
L9	VCC09
M9	VCC010
LB	VCC011
MB	VCC012
J5	VCC013
J6	VCC014
H5	VCC015
H6	VCC016

T16	GND36
T1	GND35
R15	GND34
R2	GND33
L11	GND32
L10	GND31
L7	GND30
L6	GND29
K11	GND28
K10	GND27
K9	GND26
K8	GND25
K7	GND24
K6	GND23
J10	GND22
J9	GND21
J8	GND20
J7	GND19
H10	GND18
H9	GND17
H8	GND16
H7	GND15
G11	GND14
G10	GND13
G9	GND12
G8	GND11
G7	GND10
G6	GND9
F11	GND8
F10	GND7
F7	GND6
F6	GND5
B15	GND4
B2	GND3
A16	GND2
A1	GND1

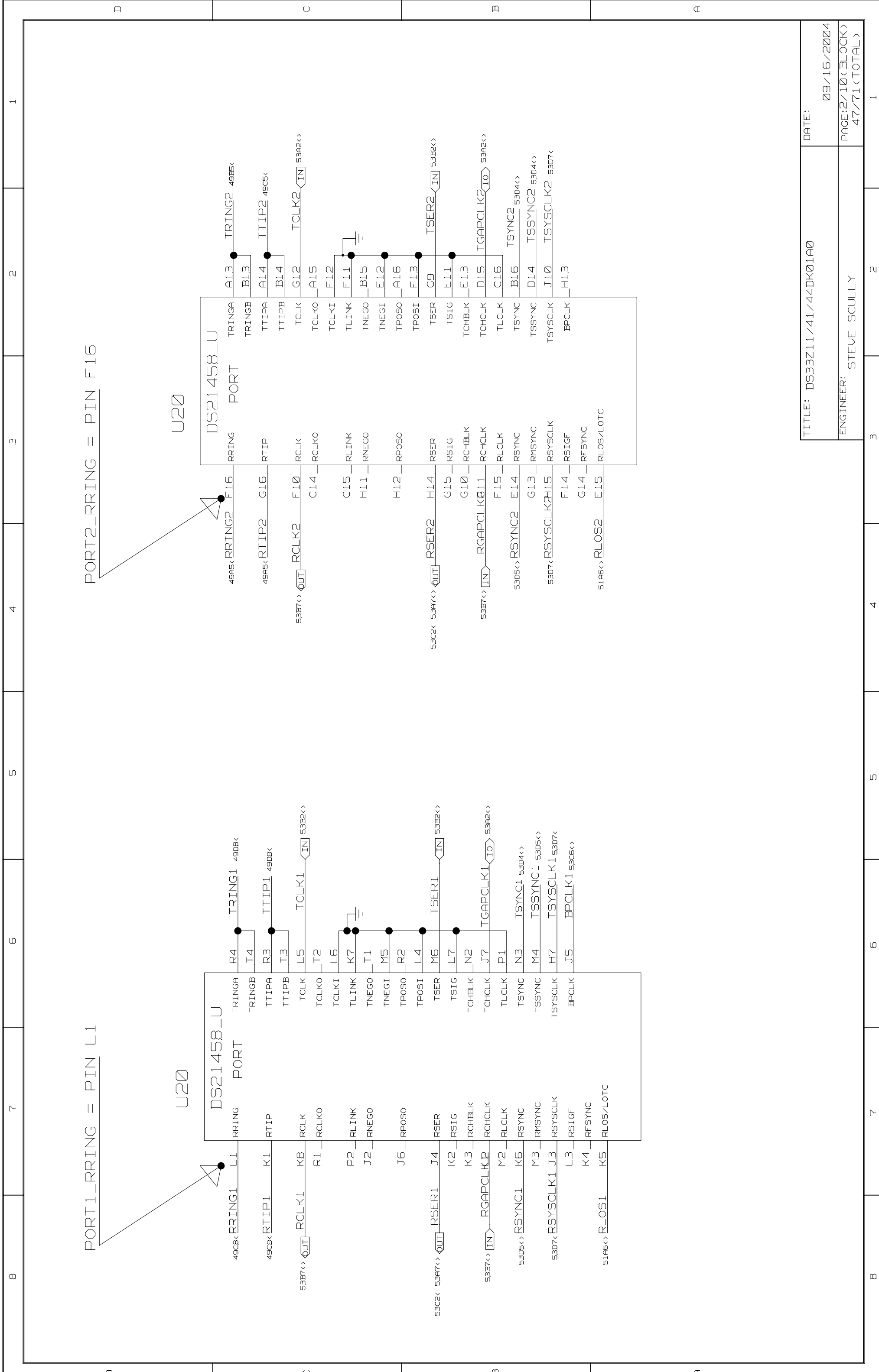
D0	CFG_DIN
D1	DNC1
D2	CLK
D3	JTD_FLASH_TDO
D4	XI_TMS
D5	ONCE_TCLK
D6	XRST
D7	CF*
D8	OE/RST*
D9	DNC2
D10	CEO*
D11	DNC6
D12	GND
D13	DNC5
D14	DNC4
D15	DNC3
D16	TDO
D17	VCCINT
D18	VCC0
D19	VCCJ
D20	CFG_DIN

P1	GND1
A16	GND2
B2	GND3
B15	GND4
F6	GND5
F7	GND6
F10	GND7
F11	GND8
G6	GND9
G7	GND10
G8	GND11
G9	GND12
G10	GND13
G11	GND14
H7	GND15
H8	GND16
H9	GND17
H10	GND18
J7	GND19
J8	GND20
J9	GND21
J10	GND22
K6	GND23
K7	GND24
K8	GND25
K9	GND26
K10	GND27
K11	GND28
L6	GND29
L7	GND30
L10	GND31
L11	GND32
R2	GND33
R15	GND34
T1	GND35
T16	GND36

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:77(BLOCK) 44/71(TOTAL)



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 46/71(TOTAL)



PORT1_RRING = PIN L1

PORT2_RRING = PIN F16

U20

U20

DS21458-U PORT

RRING	TRINGA
RTIP	TRINGB
RCLK	TTIPA
RCLKO	TTIPB
RLINK	TCLK
RNEGO	TCLKO
RPOSO	TCLKI
RSER	TLINK
RSIG	TNEGO
RCHBLK	TNEGI
RCHCLK	TPOSO
RLCLK	TPOSI
RSYNC	TSER
RMSYNC	TSIG
RSYCLK	TCHBLK
RSIGF	TCHCLK
RFSYNC	TLCLK
RLOS/LOTC	TSYNC

DS21458-U PORT

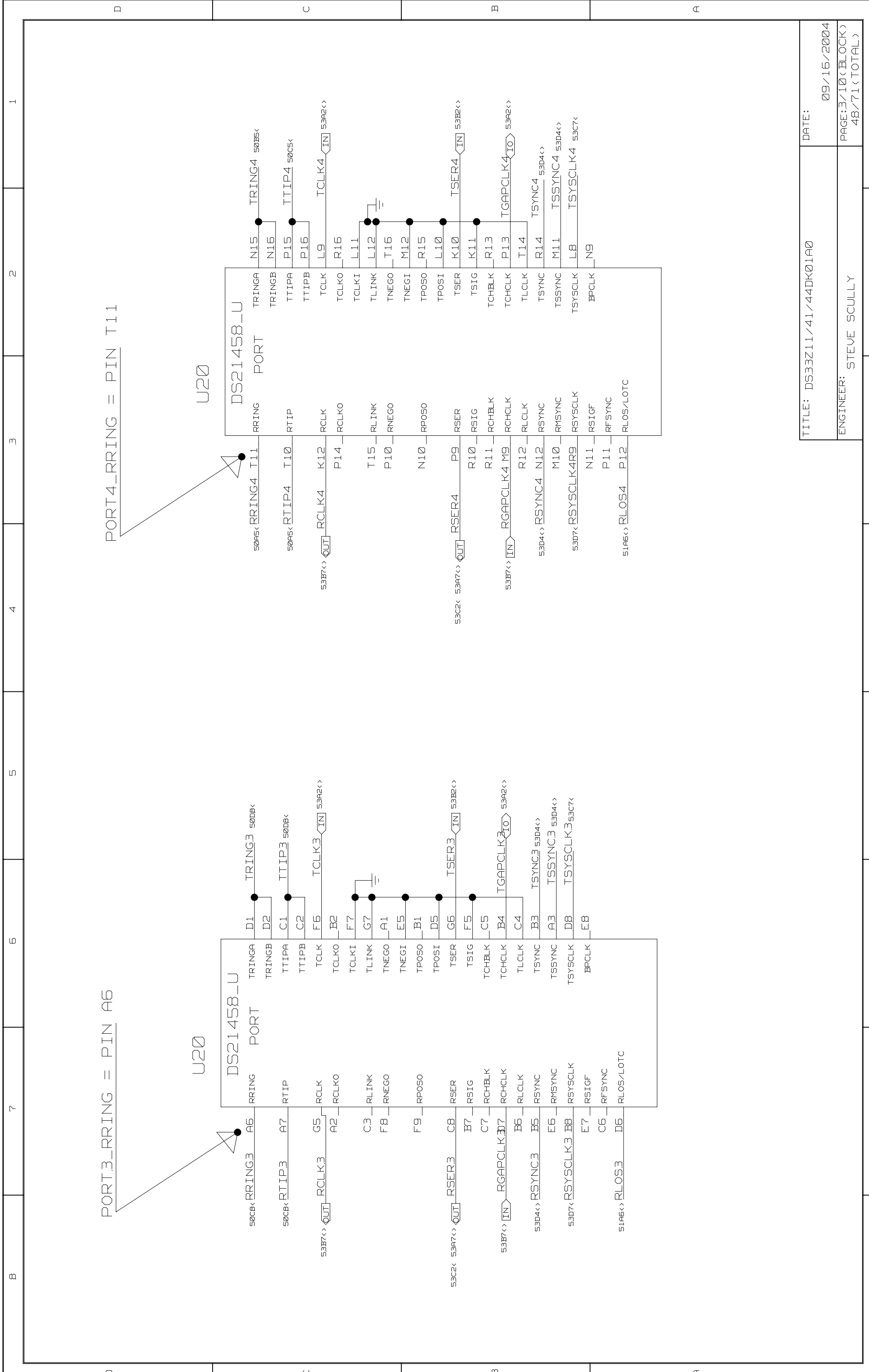
RRING	TRINGA
RTIP	TRINGB
RCLK	TTIPA
RCLKO	TTIPB
RLINK	TCLK
RNEGO	TCLKO
RPOSO	TCLKI
RSER	TLINK
RSIG	TNEGO
RCHBLK	TNEGI
RCHCLK	TPOSO
RLCLK	TPOSI
RSYNC	TSER
RMSYNC	TSIG
RSYCLK	TCHBLK
RSIGF	TCHCLK
RFSYNC	TLCLK
RLOS/LOTC	TSYNC

TITLE: DS33Z11/41/44DK01A0

DATE: 09/16/2004

ENGINEER: STEVE SCULLY

PAGE:2/10 (BLOCK)
47/71 (TOTAL)



PORT3_RRING = PIN A6

PORT4_RRING = PIN T11

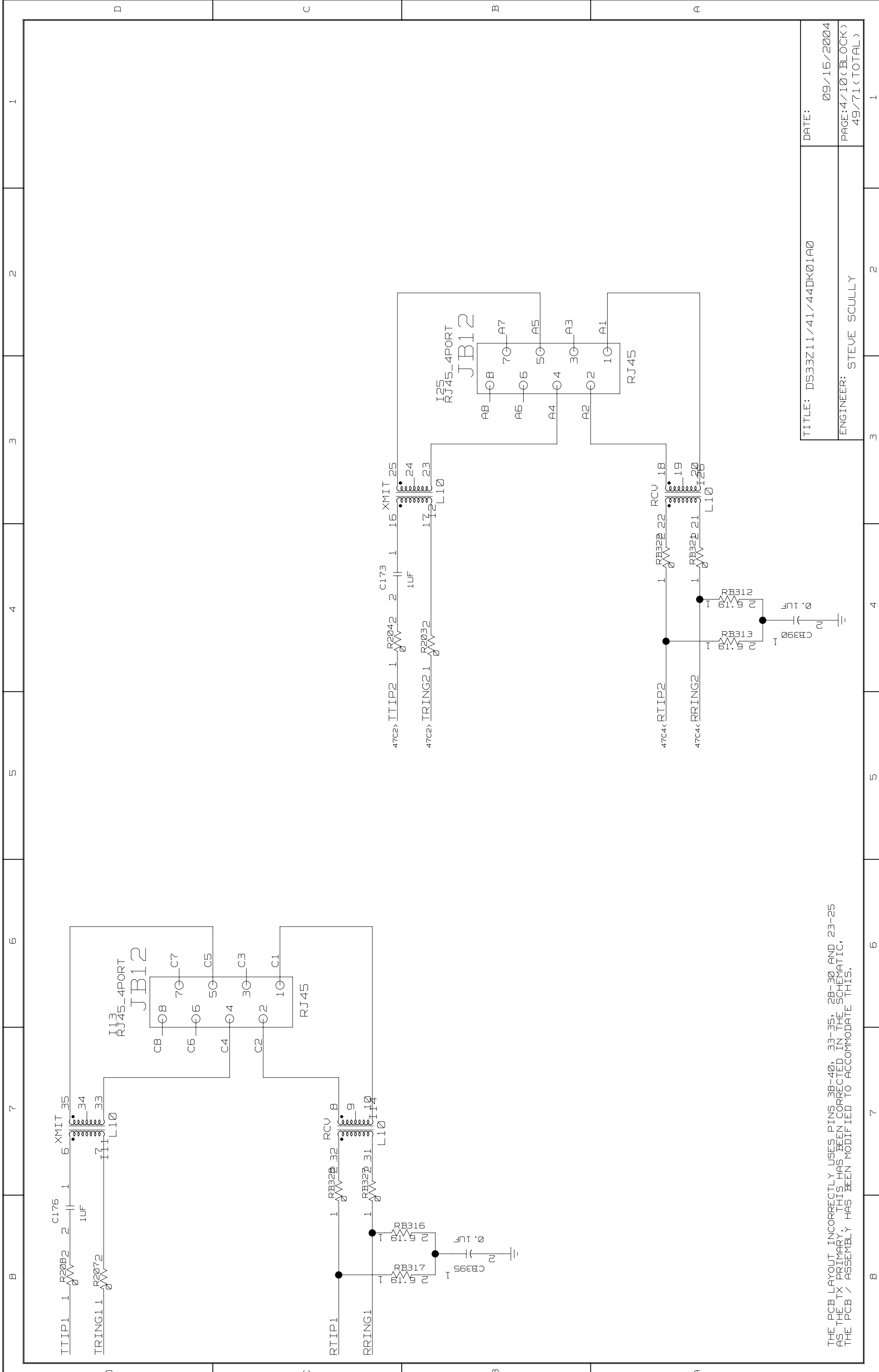
U20

U20

DS21458-U		PORT	
50C8< RRING3	A6	RRING	D1
50C8< RTIP3	A7	RTIP	D2
53B7<> OUT RCLK3	G5	RCLK	F6
	A2	RCLKO	B2
	C3	RLINK	F7
	FB	RNEGO	G7
	F9	RPOSO	A1
53C2< 53A7<> OUT RSEER3	CB	RSEER	E5
	B7	RSER	B1
	C7	RSIG	D5
53B7<> IN RGAPCLK3	B7	RCHBLK	G6
	B6	RCHCLK	F5
	B5	RLCLK	C5
53D4<> RSYNC3	B5	RSYNC	B4
	E6	RMSYNC	C4
53D7< RSYNSCLK3	B8	RSYNSCLK	B3
	E7	RSIGF	A3
	C6	RFSYNC	D8
51A6<> RLOS3	D6	RLOS/LOTC	E8

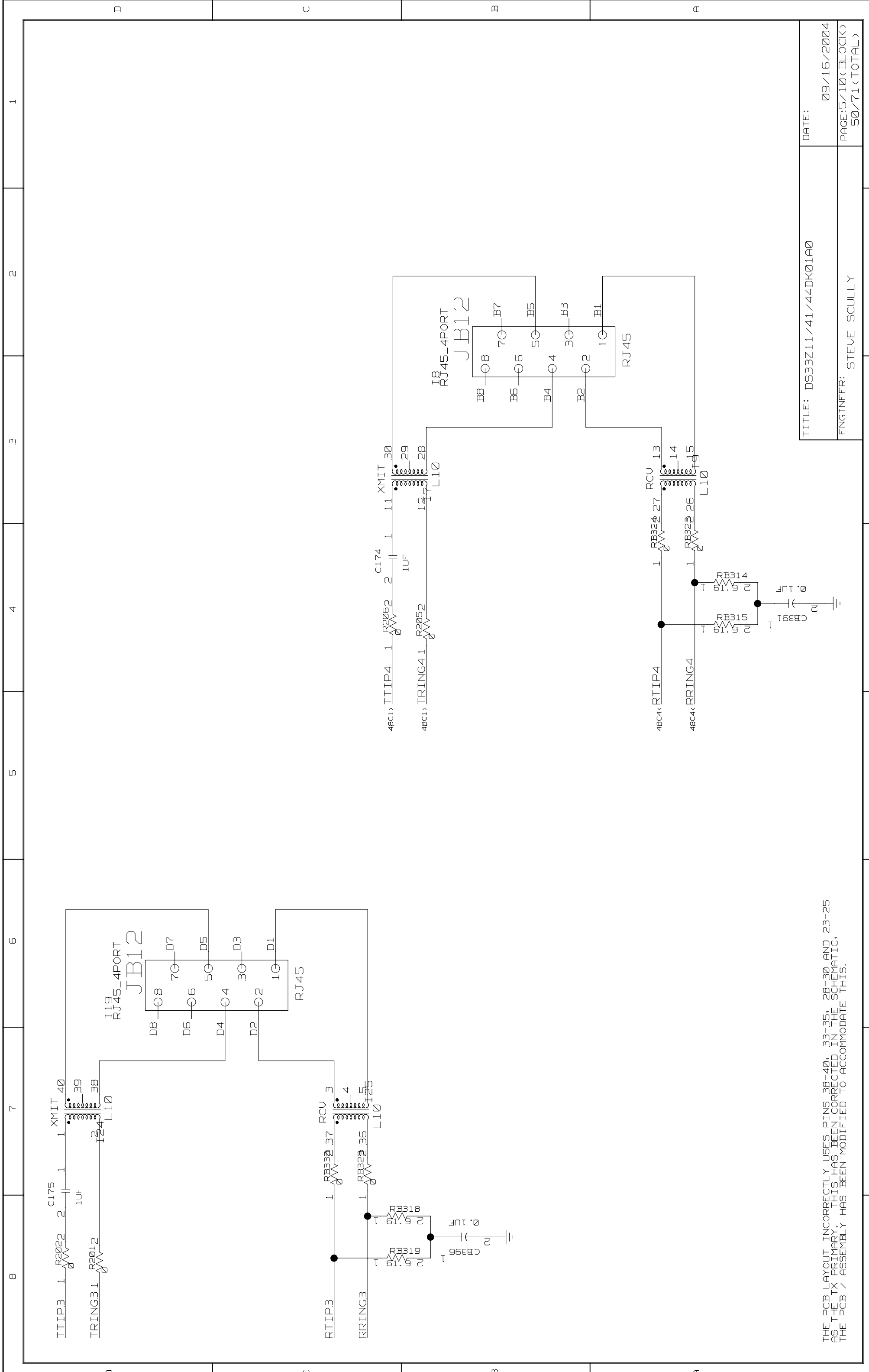
DS21458-U		PORT	
50A5< RRING4	T11	RRING	N15
50A5< RTIP4	T10	RTIP	N16
53B7<> OUT RCLK4	K12	RCLK	P15
	P14	RCLKO	P16
	T15	RLINK	L9
	P10	RNEGO	R16
	N10	RPOSO	L11
53C2< 53A7<> OUT RSEER4	P9	RSEER	L12
	R10	RSER	T16
	R11	RSIG	M12
53B7<> IN RGAPCLK4	M9	RCHBLK	R15
	R12	RCHCLK	L10
	N12	RLCLK	K10
53D4<> RSYNC4	N12	RSYNC	K11
	M10	RMSYNC	R13
53D7< RSYNSCLK4	R9	RSYNSCLK	P13
	N11	RSIGF	T14
	P11	RFSYNC	R14
51A6<> RLOS4	P12	RLOS/LOTC	M11

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:3/10 (BLOCK) 48/71 (TOTAL)



THE PCB LAYOUT INCORRECTLY USES PINS 38-40, 33-35, 28-30 AND 23-25 AS THE TX PRIMARY. THIS HAS BEEN CORRECTED IN THE SCHEMATIC. THE PCB / ASSEMBLY HAS BEEN MODIFIED TO ACCOMMODATE THIS.

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:4/10 (BLOCK) 49/71 (TOTAL)

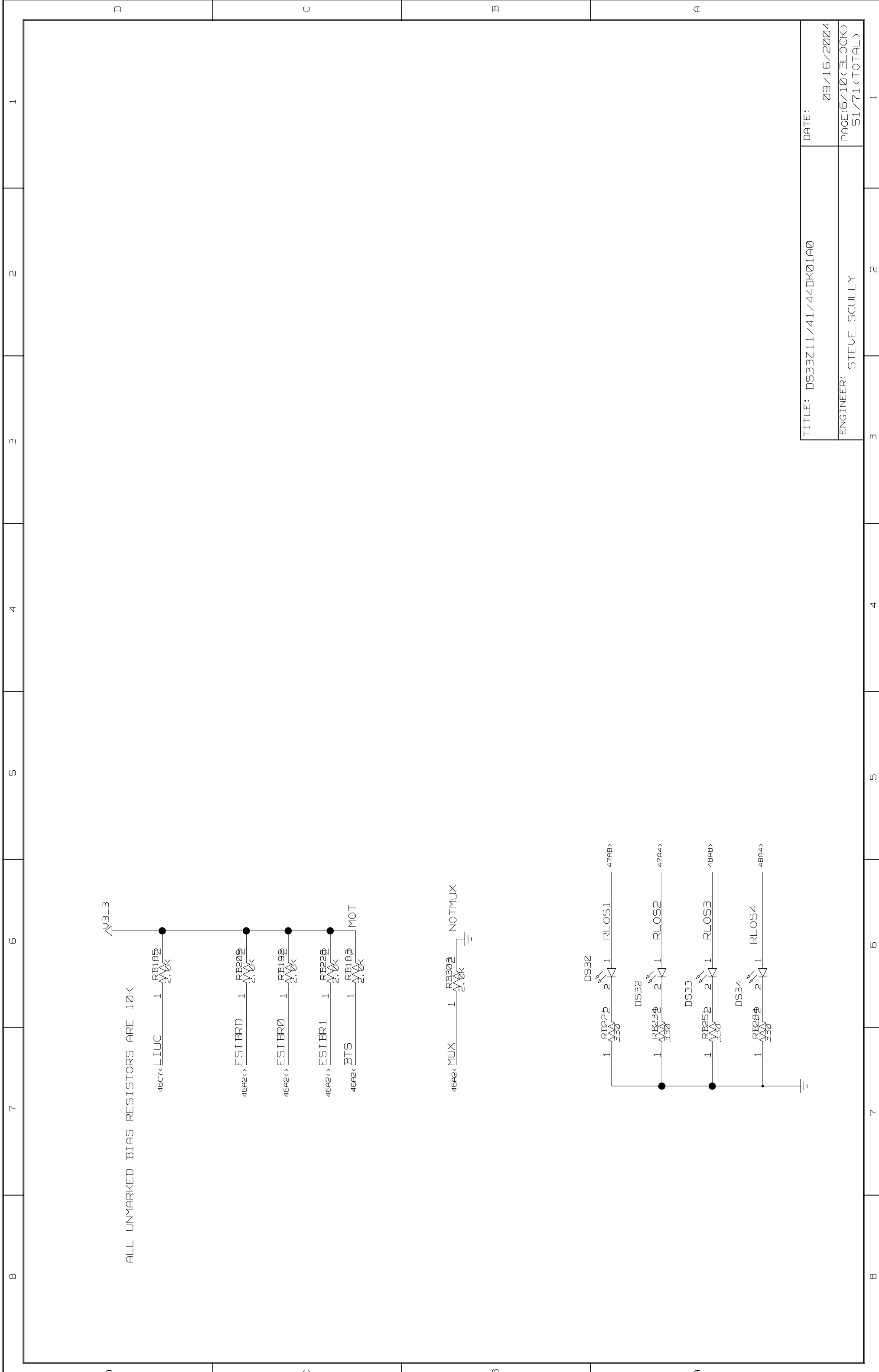


THE PCB LAYOUT INCORRECTLY USES PINS 38-40, 33-35, 28-30 AND 23-25 AS THE TX PRIMARY. THIS HAS BEEN CORRECTED IN THE SCHEMATIC. THE PCB / ASSEMBLY HAS BEEN MODIFIED TO ACCOMMODATE THIS.

TITLE: DS33Z11/41/44DK01A0

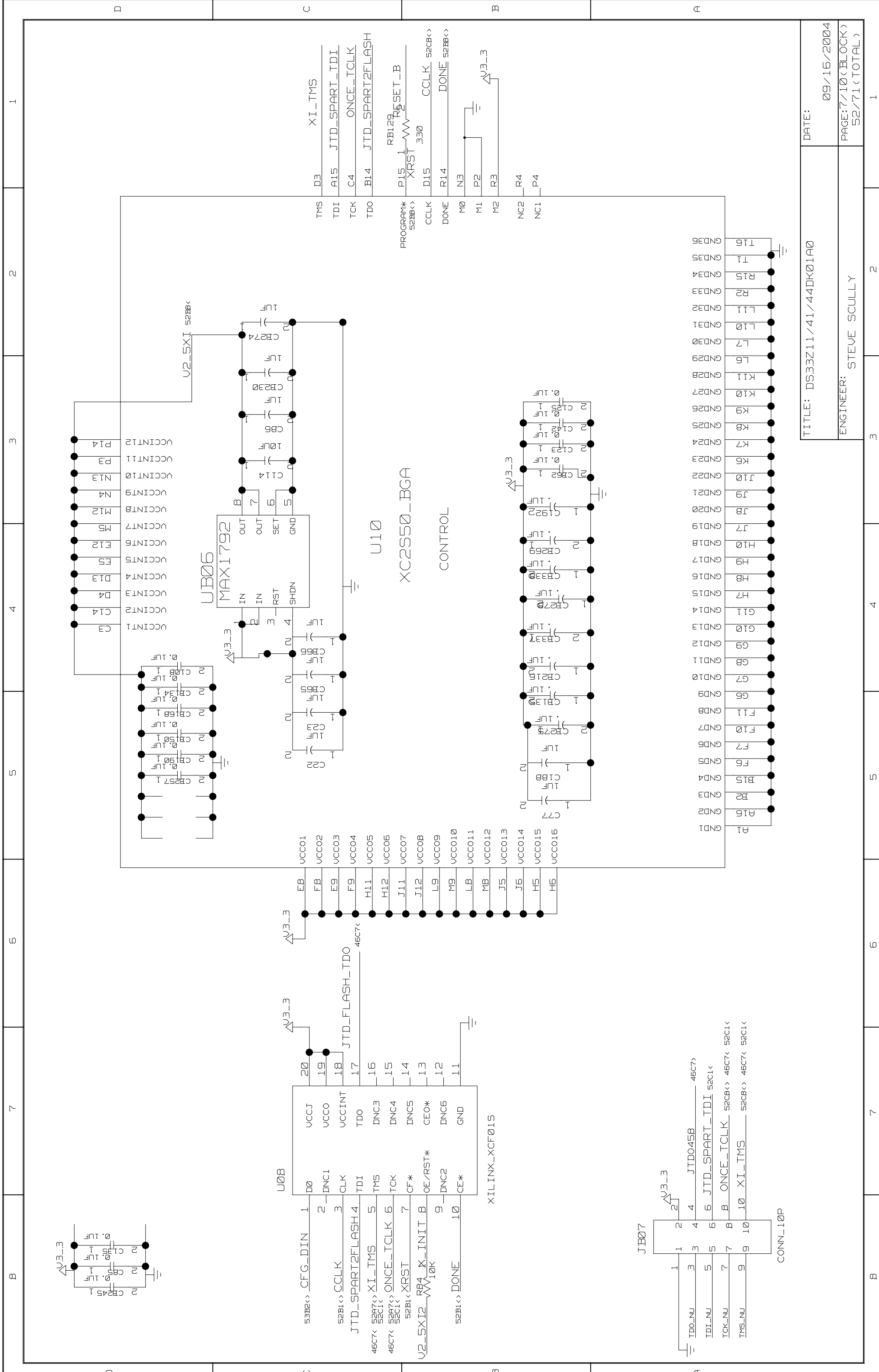
DATE: 09/16/2004

ENGINEER: STEVE SCULLY
PAGE:5/10 (BLOCK)
50/71 (TOTAL)

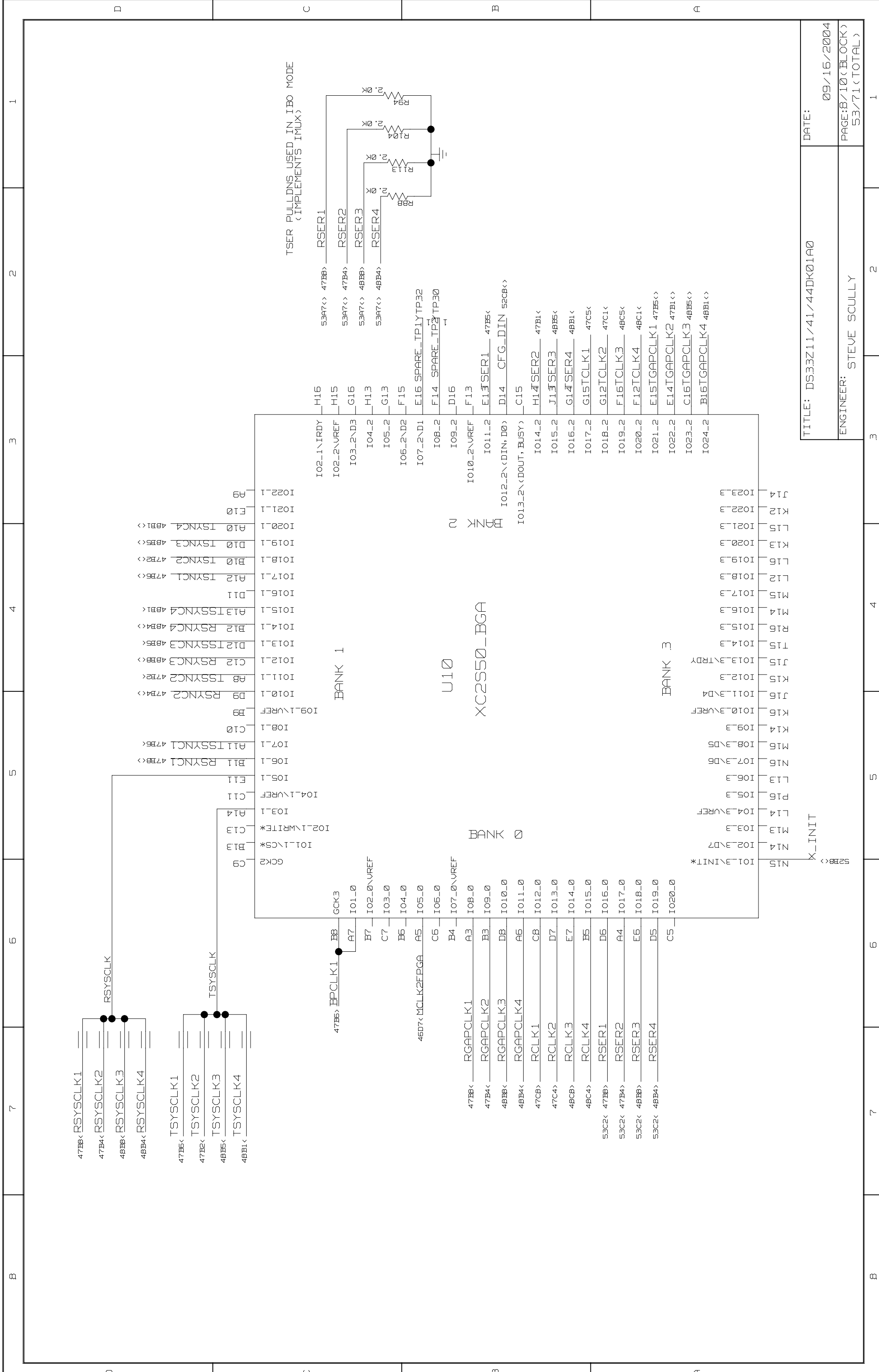


ALL UNMARKED BIAS RESISTORS ARE 10K

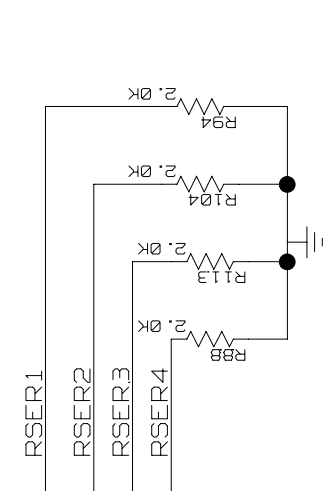
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:6/10 (BLOCK) 51/71 (TOTAL)



TITLE: DS33Z11/41/44DK01A0
 ENGINEER: STEVE SCULLY
 DATE: 09/16/2004
 PAGE: 7/10 (BLOCK)
 52/71 (TOTAL)



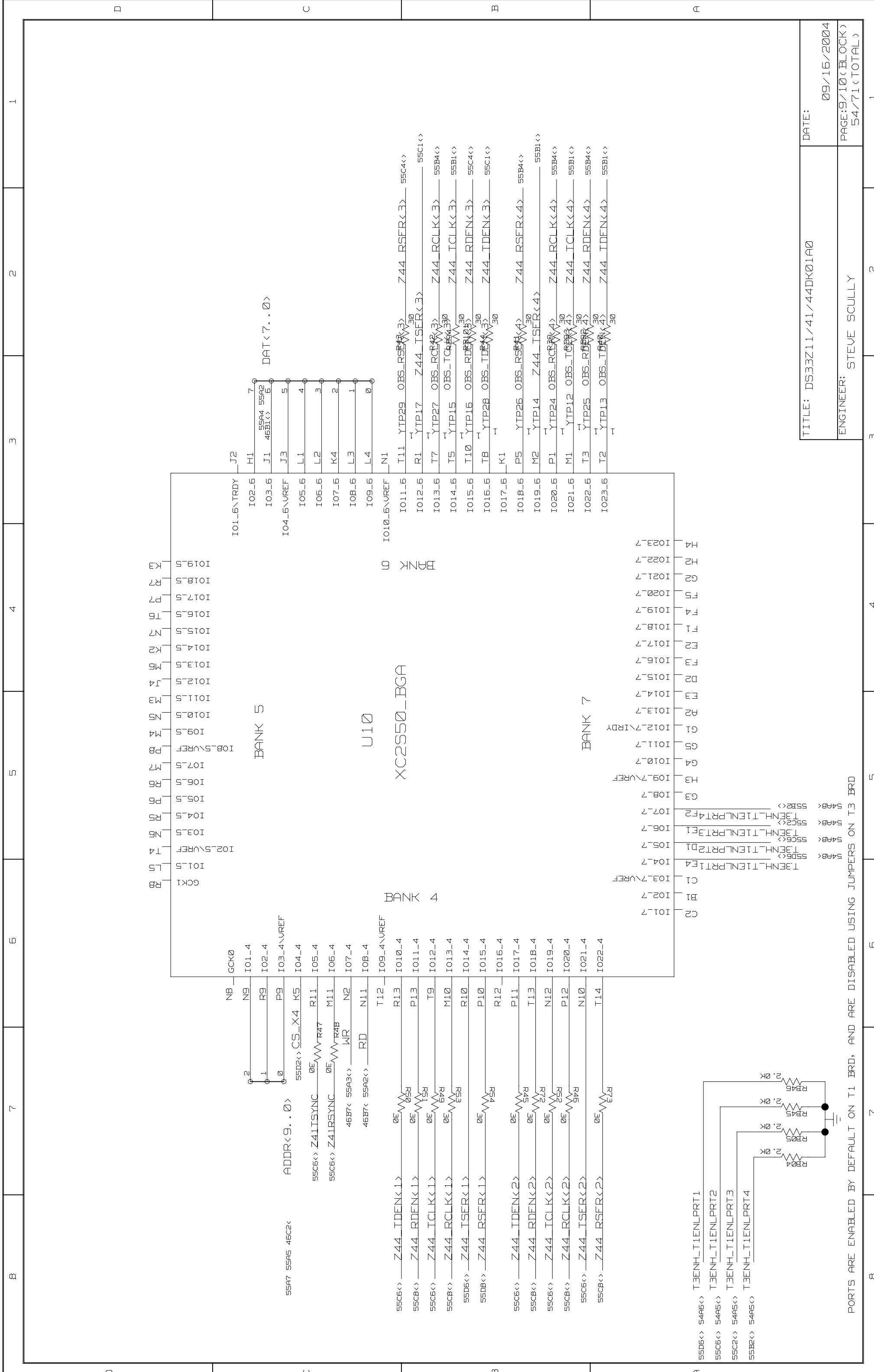
TSER PULLDWS USED IN IBO MODE
(IMPLEMENTS IMUX)



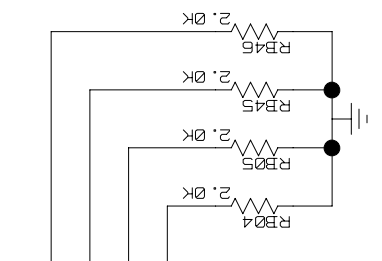
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 8/10 (BLOCK)
	53/71 (TOTAL)

B 7 6 5 4 3 2 1

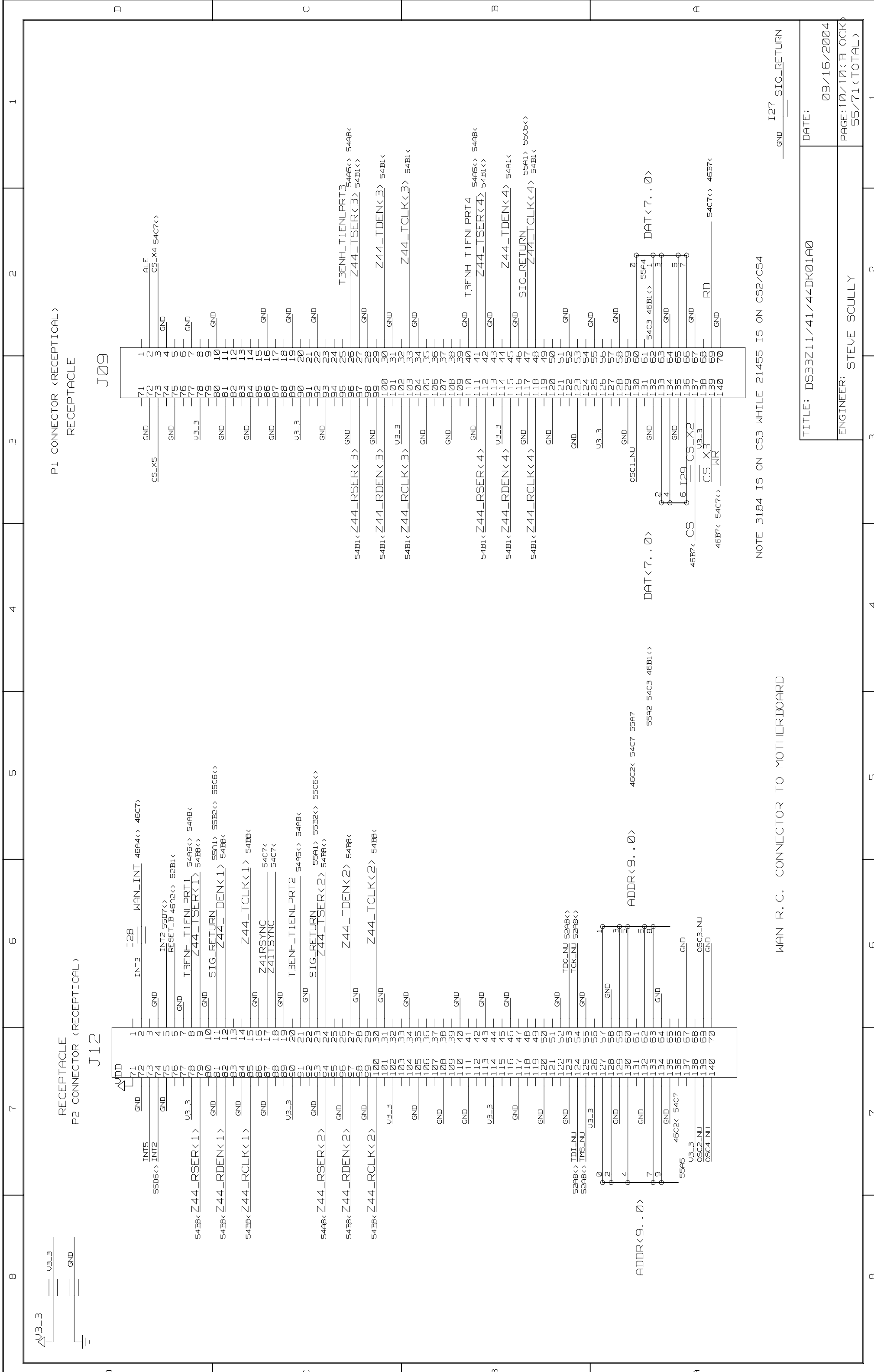
D C B A



PORTS ARE ENABLED BY DEFAULT ON T1 BRD, AND ARE DISABLED USING JUMPERS ON T3 BRD



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 9/10 (BLOCK) 54/71 (TOTAL)



NOTE 3184 IS ON CS3 WHILE 21455 IS ON CS2/CS4

WAN R.C. CONNECTOR TO MOTHERBOARD

I27 SIG_RETURN

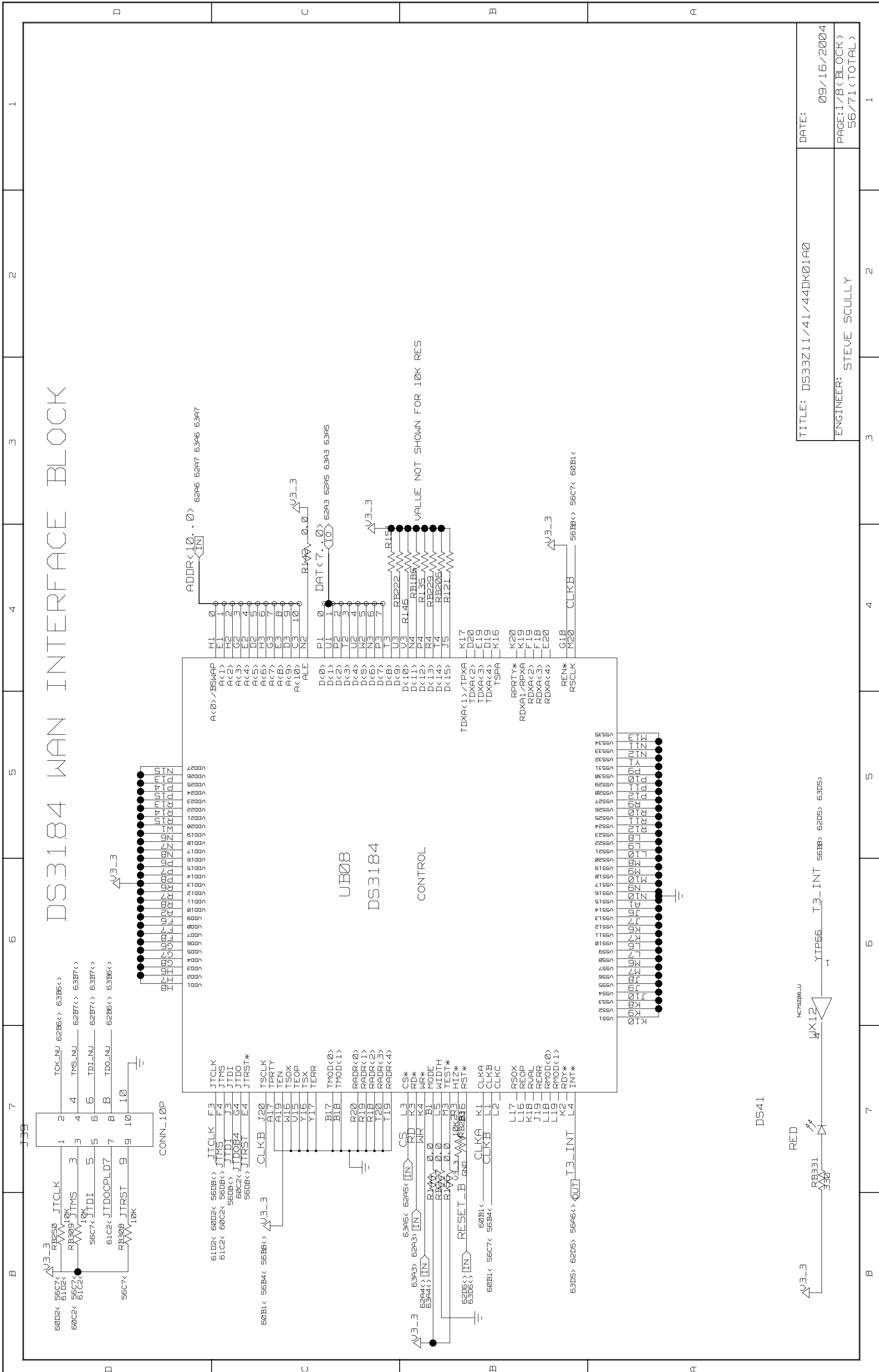
TITLE: DS33Z11/41/44DK01A0

DATE:

09/16/2004

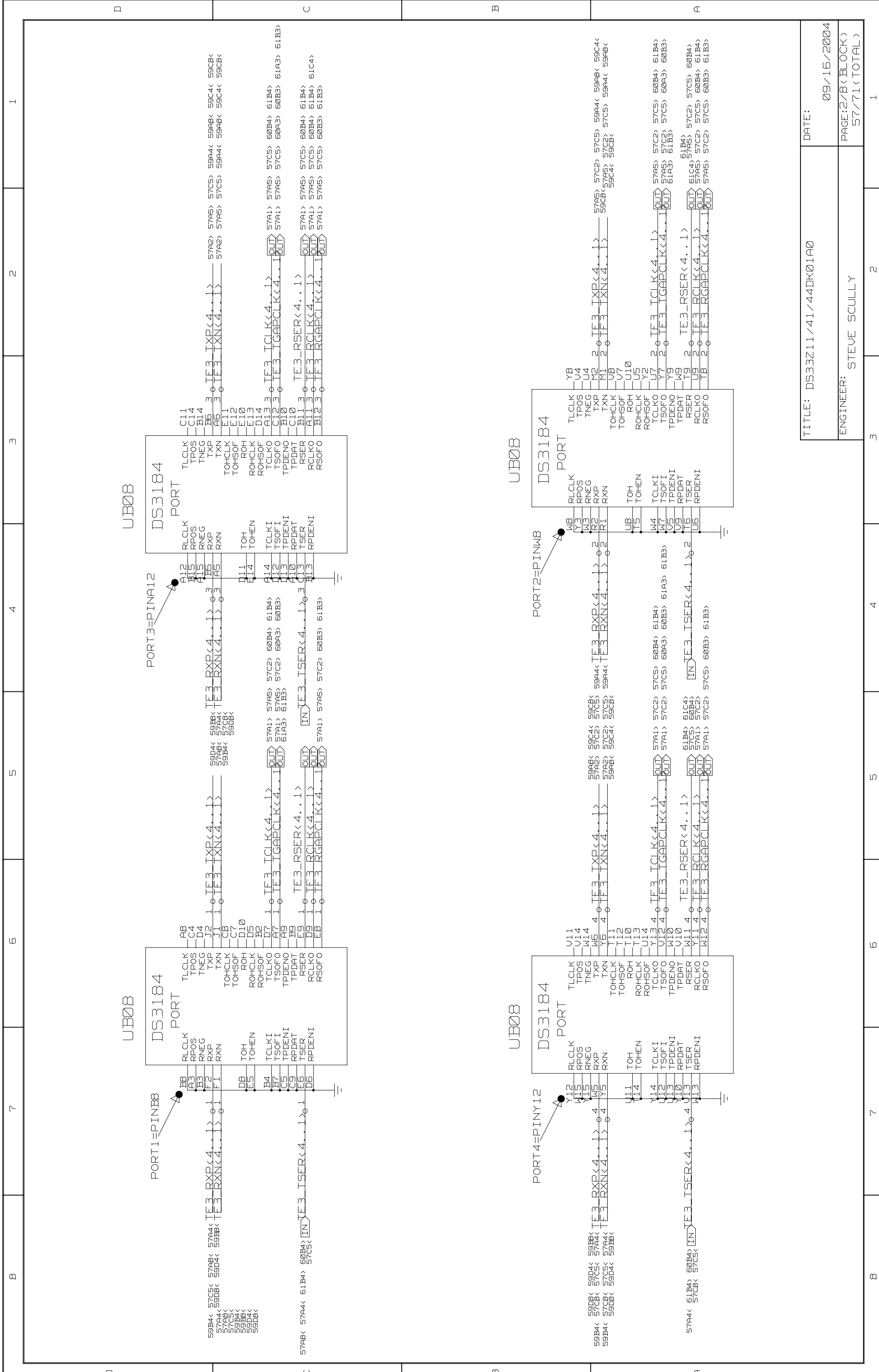
ENGINEER: STEVE SCULLY

PAGE:10/10 (BLOCK)
55/71 (TOTAL)

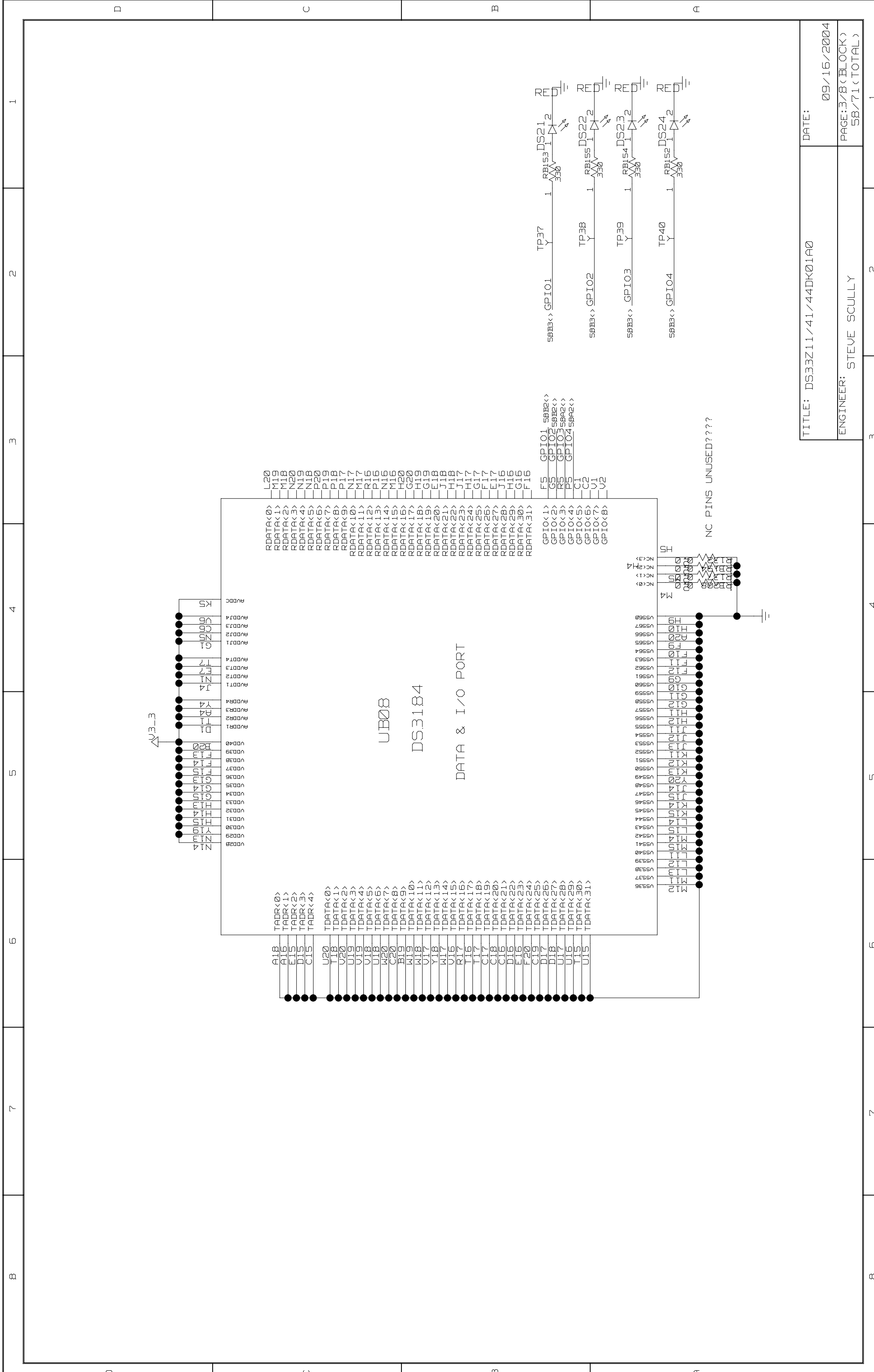


DS3184 WAN INTERFACE BLOCK

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 1/8 (BLOCK)
	56/71 (TOTAL)



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/8 (BLOCK) 57/71 (TOTAL)

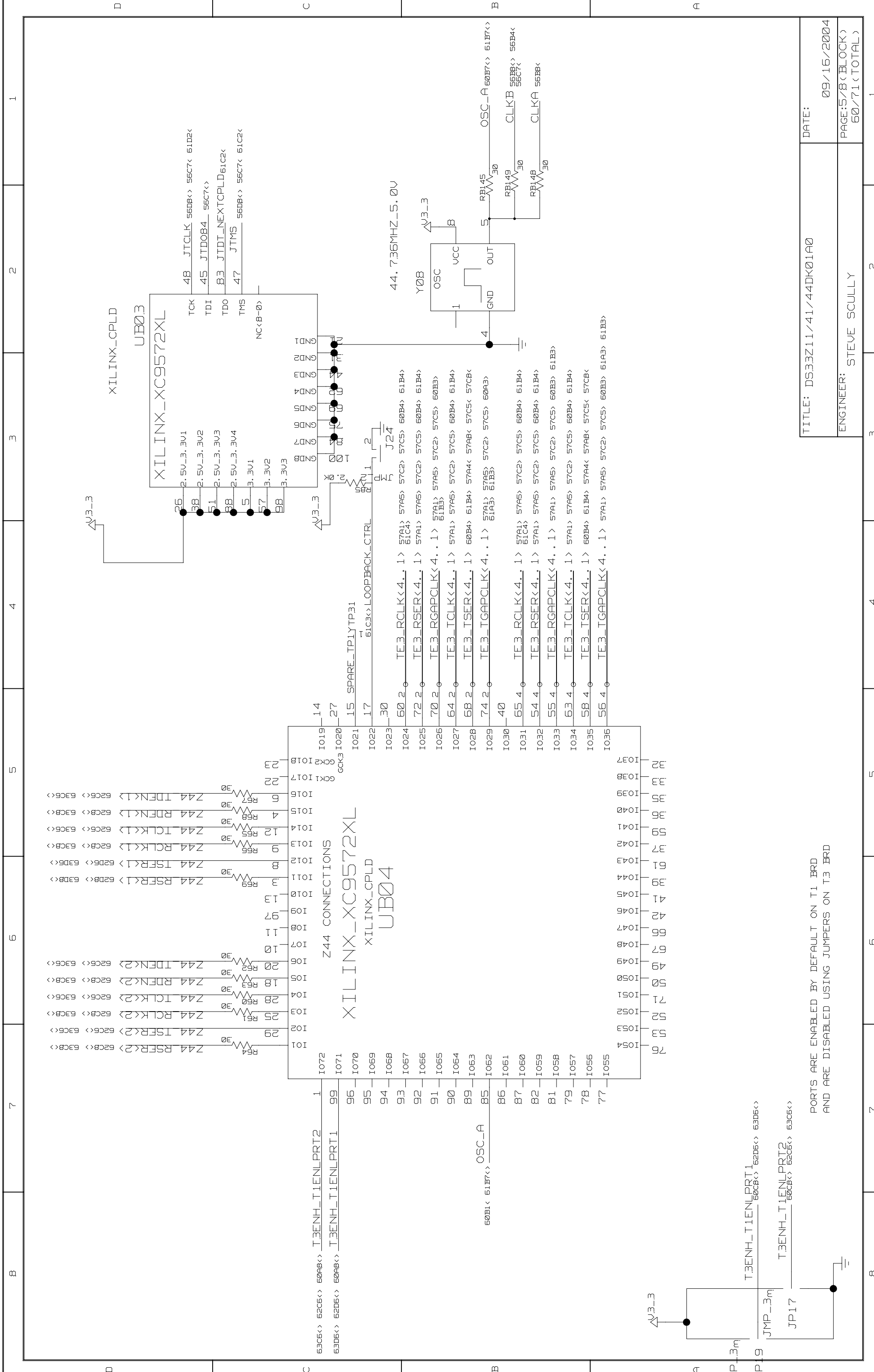


TITLE: DS33Z11/41/44DK01A0

DATE: 09/16/2004

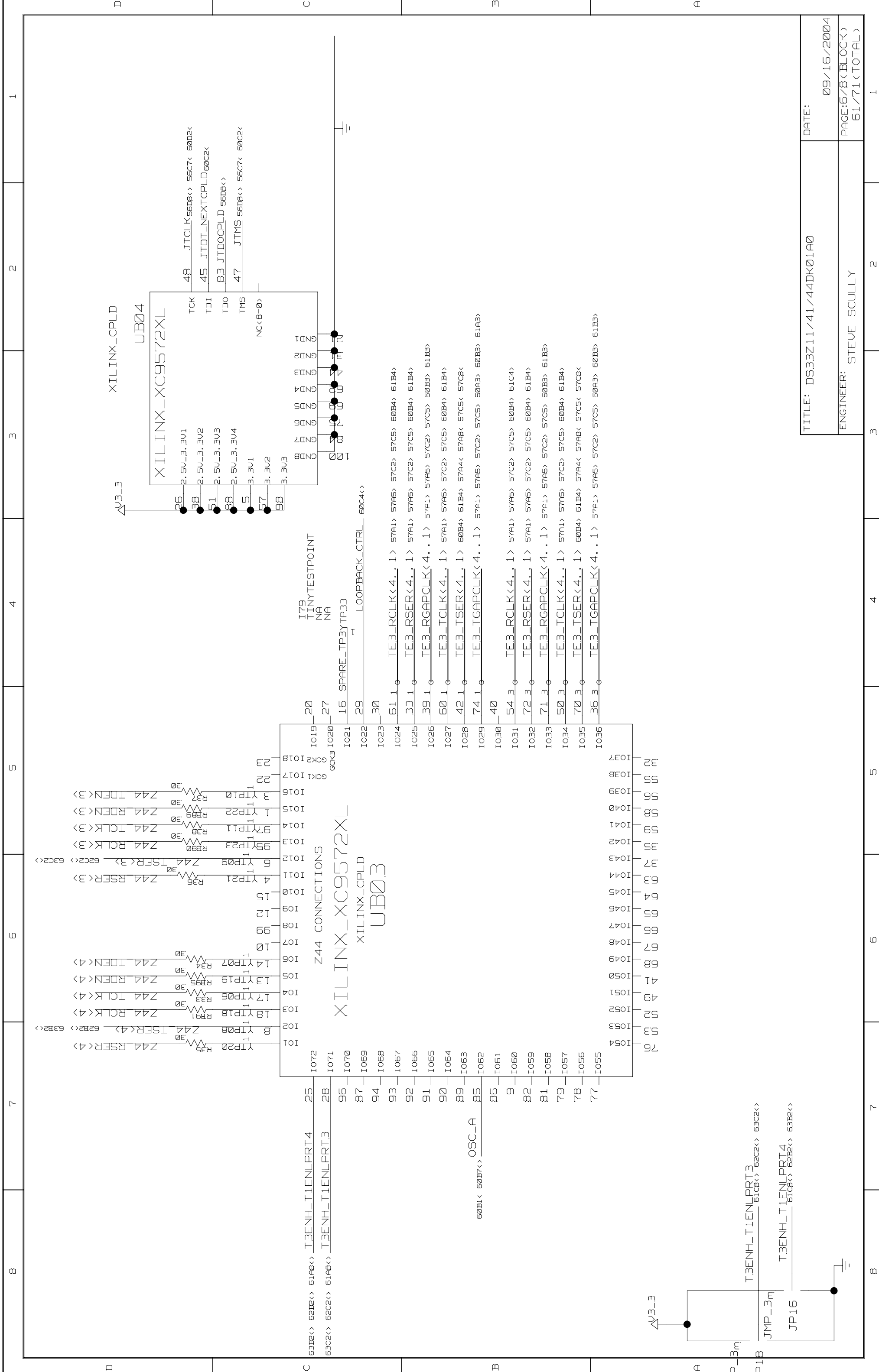
ENGINEER: STEVE SCULLY

PAGE:3/8 (BLOCK)
58/71 (TOTAL)



TITLE: DS33Z11/41/44DK01A0
 ENGINEER: STEVE SCULLY
 DATE: 09/16/2004
 PAGE: 5/8 (BLOCK)
 60/71 (TOTAL)

PORTS ARE ENABLED BY DEFAULT ON T1 BRD
 AND ARE DISABLED USING JUMPERS ON T3 BRD



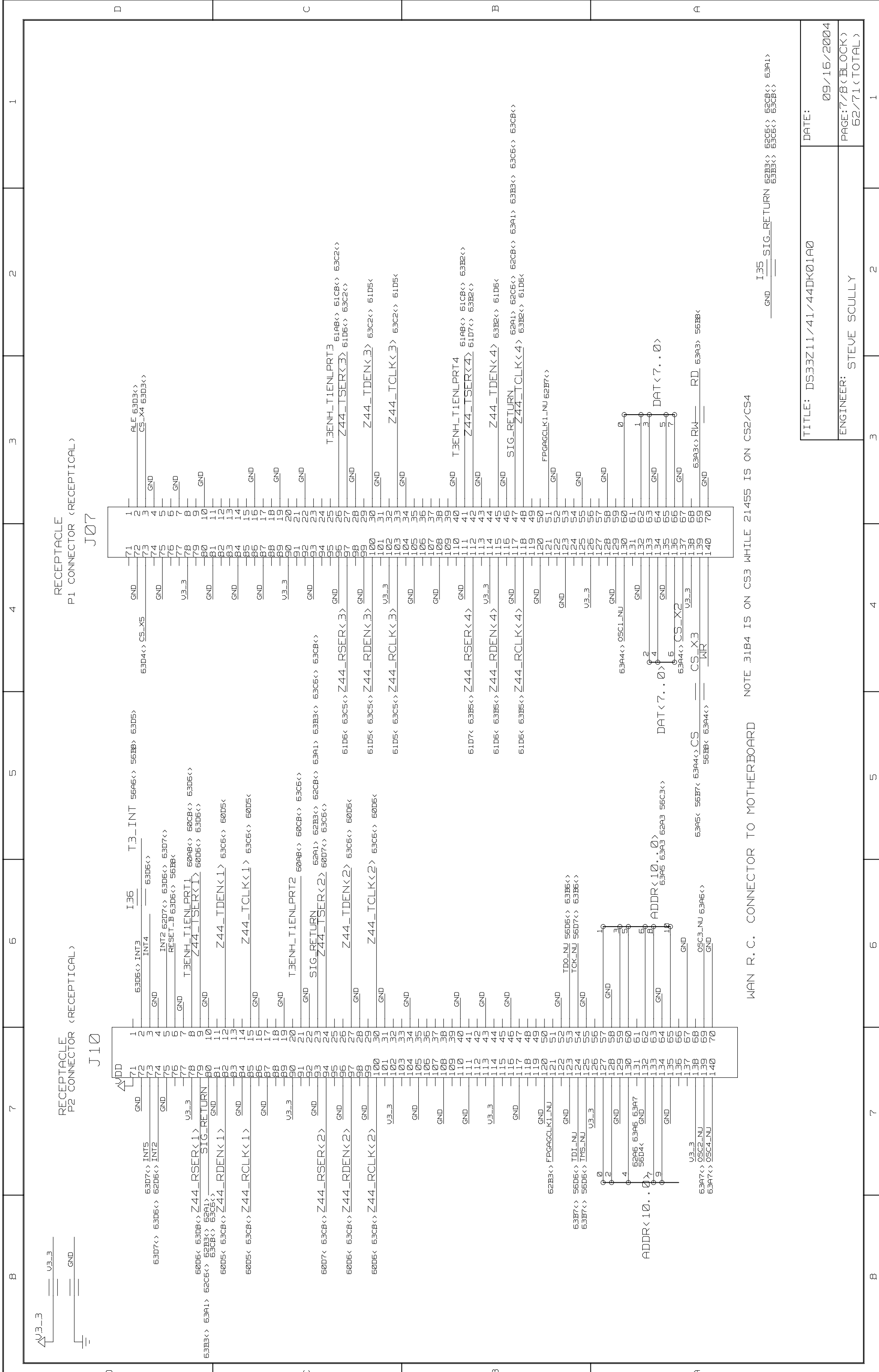
Z44 CONNECTIONS

I019	20	I072	25
I020	27	I071	28
I021	16	I070	96
I022	29	I069	87
I023	30	I068	94
I024	61	I067	93
I025	33	I066	92
I026	39	I065	91
I027	60	I064	90
I028	42	I063	89
I029	74	I062	85
I030	40	I061	86
I031	54	I060	9
I032	72	I059	82
I033	71	I058	81
I034	50	I057	79
I035	70	I056	78
I036	36	I055	77

XILINX_XC9572XL UB04

26	2.5V_3.3V1	48	JTCLK_56DB<> 56C7< 60D2<
38	2.5V_3.3V2	45	JTIDT_NEXTCPLD_60C2<
51	2.5V_3.3V3	83	JTIDOCPLD_56DB<>
88	2.5V_3.3V4	47	JTMS_56DB<> 56C7< 60C2<
5	3.3V1		
57	3.3V2		
88	3.3V3		

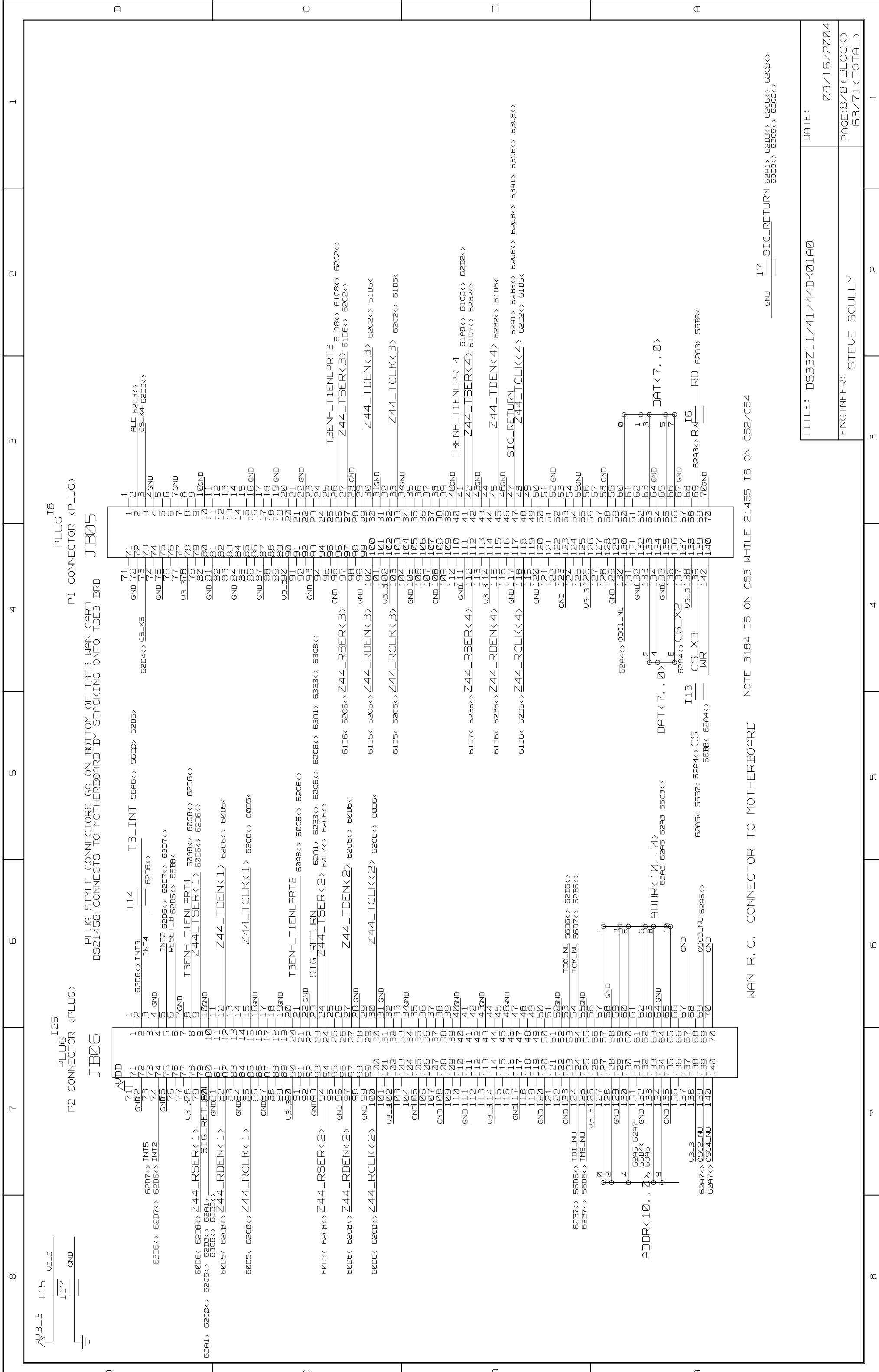
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:6/8(BLOCK) 61/71(TOTAL)



WAN R.C. CONNECTOR TO MOTHERBOARD NOTE 3184 IS ON CS3 WHILE 21455 IS ON CS2/CS4

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 7/8 (BLOCK) 62/71 (TOTAL)

I35 SIG_RETURN 62B3<> 62C6<> 63A1<> 63B3<> 63C6<> 63C8<>



TITLE: DS33Z11/41/44DK01A0
 ENGINEER: STEVE SCULLY
 DATE: 09/16/2004
 PAGE: 8/8 (BLOCK)
 63/71 (TOTAL)

WAN R.C. CONNECTOR TO MOTHERBOARD NOTE 3184 IS ON CS3 WHILE 21455 IS ON CS2/CS4